UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Juniper Networks, Inc.
Petitioner

v.

Brixham Solutions, LTD.
Patent Owner

_____

Case IPR: IPR2014-00431
Patent 7,535,895 B2

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DECLARATION OF TAL LAVIAN, PH.D. IN SUPPORT OF JUNIPER'S REPLY TO BRIXHAM'S RESPONSE TO PETITION

I, Tal Lavian, declare as follows:

1. I have personal knowledge of the facts stated in this declaration, and could and would testify to these facts under oath if called upon to do so.

I. SCOPE OF OPINION

2. I have been retained as an independent technical consultant on behalf of Juniper Networks, Inc. ("Juniper") to provide this declaration in connection with the *inter partes* review of claims 4-5 and 15-16 ("the Challenged Claims") of U.S. Patent No. 7,535,895 ("the '895 patent"). Specifically, I have been asked to consider Brixham Solutions Ltd.'s ("BSL") Patent Owner's Response, Paper No. 21 ("Response").

3. The opinions discussed below are my own. In formulating these opinions, I have reviewed a variety of materials and made use of my own personalknowledge. The materials I have relied on in formulating my opinions are identified in this report and/or in the Appendix List that was submitted with my February 11, 2014 declaration.

4. I am being paid $400 per hour in connection with my work in this case. My compensation is not contingent on my reaching any particular findings or conclusions, or any outcome of the case.

II. BACKGROUND AND QUALIFICATIONS

5. I possess the knowledge, skills, experience, training and the education to form an expert opinion and testimony in this case. A record of my background and professional qualifications was set forth in my original declaration in support of Juniper's Petition for *Inter Partes* Review, which I incorporate by reference as if set forth herein. Ex. 1003, ¶¶ 10-31. A more detailed record of my professional qualifications, including a list of patents and academic and professional publications, is set forth in my curriculum vitae attached to my original declaration as Appendix 1.

III. BASIS FOR OPINION

6. My opinions and views set forth in this declaration are based on my education, training, and experience in the relevant field, as well as the materials I reviewed in this case, and the scientific knowledge regarding the same subject matter that existed prior to the effective filing date of the '895 patent. In addition, they are informed by the legal principles outlined in my February 12, 2014 declaration. Ex. 1003 at ¶¶ 33-51.

IV. EXECUTIVE SUMMARY

7. As I explained in my original declaration, it is my opinion that the instituted ground discloses each and every limitation of the Challenged Claims.

8. I understand that BSL disputes the disclosure of only a single limitation (hereinafter referred to as the "multiprotocol limitation"):

> "wherein at least one processing engine . . . receives data to be processed by said at least one processing engine according to a first protocol within a layer and data to be processed by said at least one processing engine according to a second protocol within said layer and said first protocol is different than said second protocol."

Ex. 1004 ("Bell"). I understand that Juniper's Reply may only respond to arguments raised in BSL's Response (Paper 21). Accordingly, I only address the multiprotocol limitation below. Failure to repeat the analysis of other elements already addressed in the Petition (Paper 1) and not challenged by BSL does not mean that I waive any of these arguments.

9. It is my opinion that Bell discloses and renders obvious the multiple protocol limitation in several ways.

10. For example, Bell discloses and renders obvious a forwarding card that may receive and process "paths" of network data according to multiple protocols within a layer (e.g., ATM and Frame Relay). Indeed, Bell teaches that its forwarding cards are made with off-the-shelf components, including a plurality of off-the-shelf interface chips. Bell also teaches that the interface chips are available from various manufactures in a variety of protocols, including, for example, ATM

and Frame Relay. Bell discloses and renders obvious the use of a forwarding card that includes a plurality of interface chips of different protocols—e.g., a forwarding card with ATM and Frame relay interface chips. *See* Section V.A.1.

11. As another example, Bell discloses that each forwarding card receives and processes "network control information" according to the Ethernet protocol. This Ethernet control data is ***in addition*** to the paths of network data received by each forwarding card. Thus, even if a forwarding card in Bell were limited to receiving and processing paths of network data according to a single protocol (e.g., ATM), Bell would still disclose the multiple protocol limitation (e.g., by receiving and processing a path of ATM data and Ethernet control data). *See* Section V.A.2.

12. As yet another example, in view of the background knowledge of one skilled in the art, it would have been obvious to employ a network processor capable of processing multiple protocols on the forwarding cards of Bell. Multiple protocol network processors were well known at the time (and widely used in networking devices like Bell). Network processors were available as off-the-shelf components and could process virtually any type of protocol (e.g., ATM ***and*** Frame Relay). Moreover, multiprotocol network processors were ideally suited for Bell's forwarding cards and placing one on a forwarding card would involve nothing more than simple substitution (the existing chips on Bell's forwarding

cards for the multiprotocol network processor). The combination would yield a forwarding card that could process multiple protocols. *See* Section V.B.

13. Accordingly, Bell in view of the background knowledge of one skilled in the art renders obvious the multiple protocol limitation in this manner as well.

14. To help illustrate the arguments that are detailed below and in Juniper's reply, I have created a set of slides which is attached as Appendix A to this declaration.

V. BELL DISCLOSES AND RENDERS OBVIOUS THE MULTIPROTOCOL LIMITATION.

15. As explained below, it is my opinion that Bell discloses and renders obvious the multiple protocol limitation in several ways.

16. Before jumping into my analysis, I note that BSL has not provided any expert testimony supporting its contentions regarding the knowledge and abilities of those skilled in the art. Nor has BSL responded to any of the specific facts or arguments I raise in my original declaration. Accordingly, my opinions regarding the knowledge and abilities of those skilled in the art stand unrebutted.

A. Bell Discloses And Renders Obvious A Forwarding Card Capable Of Processing Multiple Protocols.

17. I understand that BSL does not dispute that a forwarding card that receives and processes data according to a first and second protocol within a layer

would satisfy the multiprotocol limitation. Rather, BSL contends (mistakenly, as shown below) that Bell does not disclose or render obvious such a forwarding card.

18. As shown below, Bell discloses and renders obvious a forwarding card that can receive and process data according to multiple protocols.

1. A forwarding card in Bell can receive and process "paths" of network data carrying different protocols.

19. Bell discloses a network switch that receives incoming network data containing different protocols on one or more ports of a universal port card. Bell was designed to support sending diffrent protocols in the different streams of OC-48 SONET. For instance, Bell teaches that in one embodiment, the ports of the universal port card receive incoming OC-48 SONET streams that are made up of four STS-12c "paths."[1] *See, e.g.*, Bell at 17:63-67 ("[E]ach port 44a-44d is

[1] An OC-48 SONET stream is made-up of a combination of STS-1, STS-3c and STS-12c paths. Bell at 49:15-31. Each path is made-up of multiple "time slots"—wherein a STS-1 path has a single time slot, a STS-3c path has three time slots, and an STS-12c path has 12 time slots. *Id*. An OC-48 SONET stream has 48 time slots in total. Thus, for example, an OC-48 SONET stream received at a port of the universal port card can be made-up of four STS-12c paths.

connected to a SONET optical fiber carrying an OC-48 stream."). Bell expressly discloses that each of these paths of network data may carry a different protocol:

> "Each external network connection may provide multiple streams or paths and ***each stream or path may include data being transmitted according to a different protocol over SONET. . . (e.g., ATM, MPLS, IP, Frame Relay).***"

Bell at 53:50-64; see also *id.* at 18:15-18 ("***[E]ach path within a stream may carry a data transmitted according to a different protocol***.") (emphasis added); *see also id*. at 49:36-31 ("***The same or different protocols may be carried over different paths.***") (emphasis added). Thus, for example, in one embodiment a port on the universal port cards can receive an incoming OC-48 SONET stream that contains a path of ATM data, a path of Frame Relay data, a path of IP data, and a path of MPLS data. *Id*. This is illustrated in slide 12 of Appendix A.

20. Bell allows a user to direct a particular path of network data to a specific payload extractor chip (i.e., "slice") on a forwarding card. Bell at 56:40-44 ("The user may choose which forwarding card to assign to the new path and notify the NMS. The NMS would then fill in the forward card LID in the SET, and the PPM would only determine which time slots and slice within the forwarding card to assign."); 50:17-21 ("payload extractor chip represents a 'slice'"). One skilled in the art would understand that paths of data carrying different protocols

can be assigned to payload extractor chips on the same forwarding card. For example, the path of ATM data and the path of Frame Relay data discussed above (*see* ¶ 19), can be directed to payload extractor chips 582a and 582b (respectively) on forwarding card 546c. This is illustrated in slides 13-15 of Appendix A.

21. Indeed, there is nothing in Bell that precludes paths of data carrying different protocols from being assigned to payload extractor chips on the same forwarding card. To the contrary, Bell repeatedly emphasizes that its network switch provides "flexibility in data transmission by allowing data to be transmitted from any path on any port to any port on any forwarding card." Bell at 52:10-18; *id*. at 51:9-12 ("high degree of flexibility in directing the data between any of the forwarding cards"); *see also id*. at 54:51-55 (rejecting "a fixed set of rules" and explaining that its network switch seeks to meet "the different needs of different users/customers"); *id*. at 54:57-55:3 (explaining that the switches "provisioning policy may be modified while the network device is running to allow the policy to be changed according to a user's changing need or network device system requirements").

22. Bell discloses multiple parallel routes through a forwarding card. Each route includes a number of off-the-shelf components, including an interface chip, a bridge chip, a traffic management chip, and a switch fabric chip. Bell at

51:56-52:4 (forwarding card built with off-the-shelf components); *id.* at Fig. 36B (modified and reproduced below to show exemplary routes). The interface chip is protocol specific and therefore dictates the protocol that will be handled by the route.

23. Thus, by including interface chips that process different protocols on the same forwarding card, the forwarding card will be able to process multiple protocols.

24. One skilled in the art would understand Bell to disclose forwarding cards that can include interface chips which process different protocols.

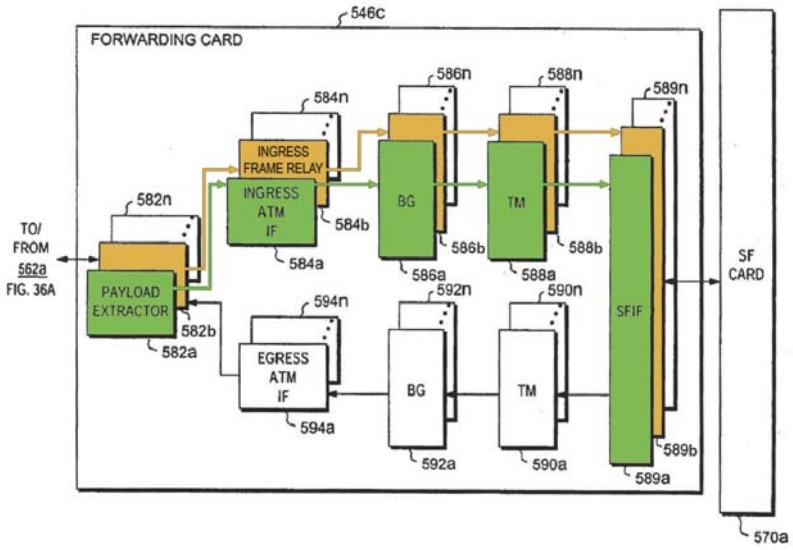
25. Indeed, in Figure 36B Bell illustrates an exemplary ingress route through a forwarding card (546c) that processes ATM data and includes an ATM interface chip. Bell makes clear that this is just "one example" and that the forwarding card can employ other types of interface chips to process other protocols:

> "The ingress interface chip will be specific to the protocol of the data within the path. ***As one example***, the data may be formatted in accordance with the ATM protocol, and the ingress interface chip is an ATM interface chip (e.g., ATM IF 584a). ***Other protocols can also be implemented*** including, for example, Internet Protocol (IP), Multi-Protocol Label Switching (MPLS) protocol or Frame Relay."

Bell at 50:36-43.

26. Thus, for example, one skilled in the art would understand Bell to also disclose a second route in the forwarding card (546c) that receives Frame Relay data at a payload extractor chip (582b) which is then processed through a Frame Relay interface chip (584b), bridge chip (586b), traffic management chip (588b), and finally to the switch fabric via a switch fabric chip (589b).

27. The illustration below is based on Figure 36B and depicts the ATM and Frame Relay routes through the forwarding card:



Bell at Fig. 36B (modified to add exemplary Frame Relay route); *see also* Appendix A, Slides 12-15.

28. In any event, it would have certainly been obvious for one skilled in the art to configure the switch of Bell so that a forwarding card processes multiple protocols. For example, it would have been obvious for one skilled in the art to

configure the forwarding card as described and illustrated in Paragraphs 20-27, such that a single forwarding card includes interface chips that process different protocols (e.g., ATM and Frame Relay). This is illustrated in slide 16 of Appendix A.

29. As previously mentioned, Bell's forwarding card, including its interface chips, are made with off-the-shelf components available from various manufacturers. Bell expressly states that these off-the-shelf components in its system can be used to implement "other protocols." Bell at 50:36-43. Thus, a person having ordinary skill in the art would have found it a matter of straightforward substitution (e.g., one type of interface chip for another) to configure a forwarding card to process multiple protocols. Moreover, substituting one type of off-the-shelf chip for another would be well within the capabilities of one skilled in the art. A person having ordinary skill in the art would also recognize that this substitution would yield the predictable result of a forwarding card that can process multiple protocols.

30. Indeed, the specifications of these off-the-shelf components were published by these manufacturers with ample examples, diagrams and reference boards on how to use them. The main job of sales engineers of these manufacturers is to show how to use these components and to sell them. One skill in the art would

easily design forwarding cards based on these components and their published interfaces. This is exactly the job of a person designing these cards.

31. One skilled in the art would have been motivated to make this simple substitution because it would further Bell's goal of "provid[ing] flexibility in data transmission by allowing data to be transmitted from any path on any port to any port on any forwarding card." Bell at 52:10-18; *id*. at 51:9-12 ("high degree of flexibility in directing the data between any of the forwarding cards"). The substitution would also further Bell's goal of meeting "the different needs of different user/customers." Bell at 54:51-55; *see also id.* at 54:57-55:3 (system "allow[s] the policy to be changed according to a user's changing need or network device system requirements").

32. Accordingly, it is my opinion that Bell discloses and renders obvious a single forwarding card that can process paths of network data carrying different protocols (e.g., ATM and Frame Relay).

2. In addition to the paths of network data, forwarding cards in Bell process Ethernet "network control information."

33. As just described above, Bell discloses and renders obvious forwarding cards that can receive and process paths of network data carrying different protocols (e.g., ATM and Frame Relay). However, even assuming Bell's forwarding cards are restricted to receiving and processing paths of network data

carrying only a single protocol (they are not), Bell still discloses the multiple protocol limitation in another manner.

34. For instance, Bell explains that each of the forwarding cards receives "network control information" over an "Ethernet control bus." Bell at 48:53-56; 49:39-42. Each forwarding card can receive and process "network control information." *Id*. at 49:41-43. "[N]etwork control information" is received from the "Ethernet control bus" and "process[ed]" by the forwarding card. *Id*. at 42-44. To receive and then process data from an Ethernet bus, it is necessary to process the Ethernet protocol. This is illustrated in slides 19-21 of Appendix A.

35. Bell makes clear that this processing of Ethernet "network control information" is ***in addition*** to processing of the paths of network data (*see* ¶¶ 19-32) received by each forwarding card at that same protocol layer. *See, e.g.*, Bell at 48:53-56 (establishing that *every* forwarding card receives and processes Ethernet network control information), 49:39-47 (same), 50:31-43 (establishing that every forwarding card *additionally* has an "ingress interface chip" for receiving and processing, e.g., "ATM" or "Frame Relay" data).

36. Accordingly, Bell discloses the multiple protocol limitation in this independent manner as well: a single forwarding card that receives and processes

(i) paths of network data according to a first protocol (e.g., ATM or Frame Relay), and (ii) network control data according to a second protocol (e.g., Ethernet).

B. It Would Have Been Obvious To Incorporate A Network Processor On The Forwarding Cards Of Bell.

37. It is my opinion that Bell in view of the background knowledge of one skilled in the art renders obvious the multiprotocol limitation. For example, as I explained in my original declaration, it would have been obvious for one skilled in the art to incorporate a "network processor" that can process multiple protocols on the forwarding cards of Bell. Thus, even if Bell does not anticipate the multiprotocol limitation (which it does), it would certainly render it obvious in view of the background knowledge of a person having ordinary skill in the art.

38. The '895 patent does not invent a new network processor. There is no enabling disclosure for such an invention. Moreover, by the time of the '895 patent, the term "network processor" referred to a well-known type of component.

39. It was common knowledge to those of skill in the art at the time that various manufacturers offered off-the-shelf network processors that could process multiple protocols. Some examples of these manufacturers are Agere Systems, Freescale, Motorola, IBM, and Applied Micro Circuits. Ex. 1003, App. 8 (Frenzel), Ex. 1003, App. 18 (Husak), Ex. 1003, App. 19 (Shah). Network processors from these manufacturers were capable of handling "virtually any type

of traffic" including, e.g., "Frame Relay," "ATM," "MPLS," and "IP." Ex. 1003, App. 8 (Frenzel) at 1-2; *see also* Ex. 1003, App. 18 (Husak) (Figure 2, showing interface cards coupled to Freescale C-5 DCP chip that processes "Frame Relay," "MPLS," "ATM," and "IP"), Ex. 1003, App. 19 (Shah) ("NPUs even have programmable peripherals to support multiple protocols," for example "Motorola DCP C-5"), Ex. 1021-2 (identifying nearly 20 network processors). Slides 26-28 of Appendix A identify some of these network processors and the protocols they process.

40. It was also common practice to use these off-the-shelf network processors within a network switch architecture like Bell. Bell itself specifically notes that the components for its network switch could be obtained from a number of vendors who sell off-the-shelf parts. Moreover, those skilled in the art understood that the "target applications" for network processors included a network switch like Bell. *See, e.g.*, Ex. 1003, App. 9 at 2 ("Target applications include multiprotocol core and edge switches"); Ex. 1003, App. 18 (Husak) at 2 ("Universal Switch-Router Line Cards Based on Network Processor"); Ex. 1003, App. 8 (Frenzel) at 1 (network switches designed to "meet the needs of those designing switches"). *See also* Appendix A, Slide 28.

41. One skilled in the art would have understood that any one of the many available off-the-shelf network processors that process multiple protocols could be used on the forwarding cards of Bell, thereby allowing a single forwarding card to process multiple protocols.

42. For example, in my original declaration I provided an example of how networks processors from Agere Systems (the "Agere Chip Sets") could be incorporated on the forwarding cards of Bell so as to render obvious the multiprotocol limitation. Agere Chip Sets were well-known at the time of Bell, and one of skill in the art would have certainly come across the Agere Chip Sets when looking for an off-the-shelf processing engine chip. Ex. 1003, App. 8 (Frenzel) at 2 (describing the "three-chip [network processor] solution" from Agere Systems, "a major player" in network processing); Ex. 1003, App. 9 (Agere Brief) at 1 (describing Agere's 10G Network Processor Chip Set). The Agere Chip Sets "handle[] virtually any type of traffic" including, e.g., "Frame relay," "ATM," and "MPLS." Ex. 1003, App. 8 (Frenzel) at 1-2; *see also* Ex. 1003, App. 9 (Agere Brief) at 2 (explaining that the Agere Chip Sets support "MPLS, IP . . . , ATM, and Frame relay" with "OC48c" physical input). Thus, by using a network processor like the Agere Chip Sets on the forwarding cards of Bell, *each* forwarding card of

Bell would then be capable of handling *any* of those protocols. App. 8 (Frenzel) at 2. *See also* Appendix A, Slides 28-31.

43. Agere and other similar chip sets manufacturers design and market these type of chips specifically to work in forwarding cards inside network devices. This is the business and this is the reason to design the chips, and sell them to companies like Cisco, Juniper and other network communications vendors.

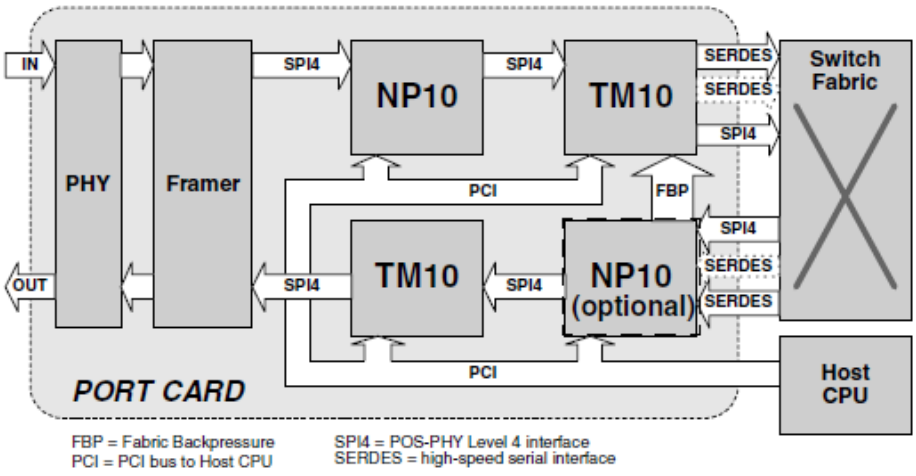
44. It would have been obvious to use the Agere Chip Sets within the Bell forwarding cards because they were ideally suited for use in the forwarding cards disclosed by Bell. For example, like the forwarding cards of Bell, the Agere Chip Sets "fits between the framer and the switch fabric." Ex. 1003, App. 8 (Frenzel) at 1; Bell at 50:2 ("framer" on port card "sends data"), 50:15-16 ("forwarding card" then "receives SONET frames"), 51:1-3 (forwarding card then "send[s] . . . to switch fabric"), Fig. 35, Fig. 36. *See also* Appendix A, Slides 29-30.

45. One skilled in the art would understand that various other off-the-shelf network processors would also fit in between the framer and switch fabric, thereby also providing an ideal fit. *See*, *e.g.*, Ex. 1003, App. 8 (Figure 1: illustrating architecture "used in most switches, routers, and other networking equipment," wherein "network processor" is placed between "framer" and "switch fabric"). The fact that the network processors like the Agere Chip Sets could have been

easily substituted for the similar component disclosed in Bell is further evidence that one of ordinary skill would easily recognize these network processors could be readily employed within the forwarding cards of Bell.

46. Indeed, the primary applications of many prior art network processors (including, for example, the Agere Chip Sets) were strikingly similar to the disclosed architecture of Bell's forwarding cards. An example of the Agere Chip Sets is shown below:

Ex. 1003, App. 9 (APP750 Brief) at 1. In this graphic, the ingress and egress



10G Network Processor System Diagram

"traffic manager (TM10)" chips and ingress and egress "classification engine (NP10)" chips are sandwiched between an external "Framer" to left and "Switch fabric" to right (which are not part of the Agere Chip Set). Thus, the Agere Chip

Sets are remarkably similar to the structure of the forwarding card disclosed in Bell:

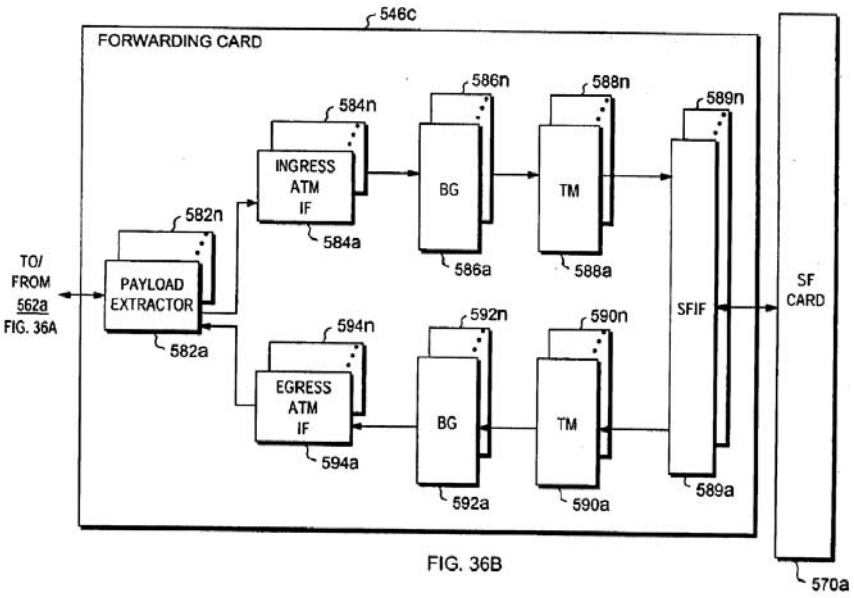


FIG. 36B

Bell at Fig. 36B. Just like in the Agere Chip Sets example, this figure depicts the ingress and egress traffic management ("TM") chips, ingress and egress protocol interface ("IF") chips, and bridge chips ("BC") which merely "serve[] as an interface" for the traffic management chips—all of which are sandwiched between an external framer to the left, and an external switch fabric to the right. *Id*. at 50:54-61 (traffic management chips), 50:36-43 (protocol interface chips), 50:50-53 (bridge chip), 49:67-50:5 (framer to left), 51:1-3 (switch fabric to right). *See also* Appendix A, Slides 28-30.

47. Moreover, implementing a network processor on the forwarding cards of Bell would be straightforward and yield predictable results. For example, it was

well within the capability of one skilled in the art to substitute a network processor like the Agere Chip Sets onto the forwarding card of Bell in place of the existing interface, bridge, and traffic management chips. Moreover, the Agere Chip Sets (as well as many other network processors) were particularly easy to program. *See, e.g.*, Ex. 1003, App. 8 (Frenzel) at 1 ("Only six lines of code, for example, are needed to implement a simple IPv4 router using the Agere chip set"—as opposed to "several hundred lines of code" required by alternative prior art chips); Ex. 1003, App. 9 (Agere Brief) at 2 (Multiprotocol customer-programmable classification"; "Uses high-level network processor programming languages—Functional Programming Language (FPL) and Agere Scripting Language (ASL)"; ("Programmable packet modification"); *see also* Ex. 1003, App. 18 at 2 ("Network Processor's Seven Key Attributes . . . A simple programming model"). As a result, any particular functions required by the Bell forwarding card could be readily programmed.

48. Thus, implementing a network processor capable of processing multiple protocols (e.g., the Agere Chip Sets) within a forwarding card of Bell would have been obvious to one skilled in the art, and the resulting system would embody the multiple protocol limitation. For example, a forwarding card would

receive and process at least ATM and Frame Relay data. Ex. 1003, App. 8 (Frenzel) at 1.

49. In addition to the reasons mentioned above, various other rationales also support my conclusion that Bell in view of the background knowledge of one skilled in the art renders obvious the multiprotocol limitation. These limitations are discussed below and in Slides 32-45 of the Appendix A.

50. For example, it would have been obvious for Bell's forwarding cards to employ a multiprotocol network processor because the combination would merely involve combining prior art elements according to known methods to yield predictable results. As already explained, at the time of Bell there were a number of different options in terms of network processors that could be used within a broader network architecture to process multiple protocols. As also explained, it would have been straightforward for a person having ordinary skill in the art to implement any one of these network processors on the forwarding cards of Bell using standard network design techniques. The combination would lead to the predictable result of a forwarding card that can process multiple protocols. In such a combination, the network processor would continue to perform its function of receiving and processing data according to multiple protocols, and the rest of the combined device would retain its function as a network switch (per Bell).

51. As another example, employing a network processor capable of processing multiple protocols on the forwarding cards of Bell would have involved nothing more than the simple substitution of one known element [e.g., the interface, bridge, and traffic management chips] for another [e.g., the Agere Chip Sets]. Indeed, as I have already explained, prior art network processors capable of processing multiple protocols were ideally suited for use in the forwarding cards disclosed by Bell. Indeed, network switches like Bell were the "target applications" for these network processors. *See, e.g.*, Ex. 1009-2. It was also well within the capabilities of one skilled in the art to substitute the existing off-the-shelf chips on Bell's forwarding cards for off-the-shelf network processors like, for example, the Agere Chip Sets, as I explained above. Doing so would yield the predictable result of a forwarding card that could process multiple protocols. The network processor would continue to perform its function of receiving and processing data according to multiple protocols, and the rest of the combined device would retain its function as a network switch (per Bell).

52. As another example, employing a network processor capable of processing multiple protocols on the forwarding cards of Bell would have involved nothing more than the use of a known technique to improve similar devices in the same way. By the time of the alleged invention, network processors were widely

used to improve devices like Bell (e.g., other switches and routers). *See, e.g.*, Ex. 1003, App. 18 at 2 ("Network Processors Are the New Approach"); Ex. 1003, App. 8 (describing various off-the-shelf network processors that could be used to "improve[]" network switches like Bell); Ex. 1003, App. 9 (describing Agere's off the-shelf "Network Processor Chip Set" whose "target applications include multiprotocol core and edge switches"). For example, network processors like the Agere Chip Sets, were used to provide flexible support for multiprotocol processing and to increase the line speeds network switches could handle. Ex. 1003, App. 8 at 2 (problem is that an "ASIC is fixed, and it can't be easily changed to support new protocols" and the "network processor was developed to solve this problem."); *id*. at 1-2 (explaining that "[e]arlier generations of NPs . . . were inadequate for line speeds greater than about OC-12," but current NPs, like those from "Agere Systems," are capable of supporting speeds of, e.g., SONET "OC-48" and "OC-192."). One skilled in the art could have applied this known technique (i.e., the use of a network processor capable of processing multiple protocols) to the network switch of Bell to achieve the predictable results of that combination (a forwarding card capable of processing multiple protocols).

53. As another example, employing a network processor capable of processing multiple protocols on the forwarding cards of Bell would merely be

applying a known technique (i.e., the use of a network processor capable of processing multiple protocols) to a known device ready for improvement (i.e., the network switch of Bell) to yield predictable results and an improved system (a flexible network switch that can efficiently handle any type of protocol). Ex. 1003, App. 18 at pg. 2 ("Network Processor's Seven Key Attributes"); Ex. 1003, App. 8 at 1 ("network processor was developed to" allow a designer to easily "support new protocols," or "add new functions").

54. As another example, employing a network processor capable of processing multiple protocols on the forwarding cards of Bell would also be obvious to try. By the time of the '895 patent, network switches like that disclosed in Bell needed to be able to process various protocols. There were a finite number of ways to go about achieving this goal, each of which was predictable and provided a reasonable expectation of success. For example, a network switch could: (1) include a protocol-specific processing engine for each protocol the network switch must handle, or (2) include processing engines that could handle multiple protocols. Those of ordinary skill in the art would recognize the viability of selecting any of these discrete options.

55. As another example, work on network processors capable of processing multiple protocols would have prompted predictable variations in the

field of networking devices (including for the network switch of Bell), based on design incentives and other market forces (such as a desire for a network switch that can efficiently handle different protocols). By the time of the '895 patent, efforts to improve network processors so as to allow network switches to efficiently handle various different protocols was widespread. *See, e.g.*, Ex. 1003, App. 8 at 1-2 ("Network Processors Evolve To Meet Future Line Speeds); *id.* (problem is that an "ASIC is fixed, and it can't be easily changed to support new protocols" and the "network processor was developed to solve this problem."); *see also* Ex. 1021-8 ("it seems every month a new network process is announced. In an attempt to alleviate the bandwidth bottleneck, numerous solutions have emerged."). As previously explained, the implantation of these network processors on the forwarding cards of Bell was predictable and well within the ability of those of skill in the art.

56. Bell and the knowledge generally available to one of ordinary skill in the art also provide the teachings, suggestions, and motivations to employ a network processor capable of processing multiple protocols on the forwarding cards of Bell. By the time of the '895 patent, network processor technology was widely popular and the benefits of employing a network processor in a multiprotocol network switch like Bell were well understood. *See, e.g.*, Ex. 1003,

App. 18 at 2 ("Network Processors Are The New Approach," "Network Processor's Seven Key Attributes"); Ex. 1003, App. 8 1-2 (network processor solves the problem of fixed systems that "can't be easily changed to support new protocols"); Ex. 1003, App. 9 at 2; Ex. 1021-7 ("Network Processor (NP), provides the right balance of hardware and software"). Indeed, one skilled in the art would be unable to avoid reading about the many benefits of employing a network processor in a network switch like Bell in one of many articles and product briefs available at the time. *Id*. One skilled in the art would also understand that network processors were specifically designed to be used with a network switch like Bell. *See, e.g.*, App. 9 at 2 ("target applications include multiprotocol core and edge switches"). Moreover, one skilled in the art would recognize that employing a network processor on the forwarding cards of Bell to process multiple protocols would further Bell's stated goals of providing (1) a "high degree of flexibility in directing the data between any of the forwarding cards," and (2) "flexibility for future network device changes or the different needs of different user/customers." Bell at 51:9-12; *id*. at 54:53-55. Indeed, one of the major advantages of a network processor is that it provides "maximum system flexibility" and "complete programmability." Ex. 1003, App. 18 at 2; *see also* Ex. 1003, App. 8 at 1-2 ("Network Processor was developed to" allow designers to easily "support new

protocols, add new functions, or be easily revised to handle unexpected changes or upgrades."). Thus, one skilled in the art would recognize that a network processor would be a natural fit for the network switch of Bell.

57. In sum, it is my opinion that the multiprotocol limitation is obvious because Bell in view of the background knowledge of one skilled in the art renders obvious incorporating network processors on the forwarding cards of Bell.

VI. CONCLUSION

For the reasons stated herein, it is my opinion that the instituted grounds disclose and render obvious the multiprotocol limitation. This declaration is based on my present assessment of materials and information currently available to me. My investigation and assessment may continue, which may include reviewing documents and other information that may yet be made available to me. Accordingly, I expressly reserve the right to continue my study in connection with this case and to expand or modify my opinions and conclusions as my study continues.

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Respectfully submitted,

Dated: Dec 19th, 2014

By: Tal Lavian

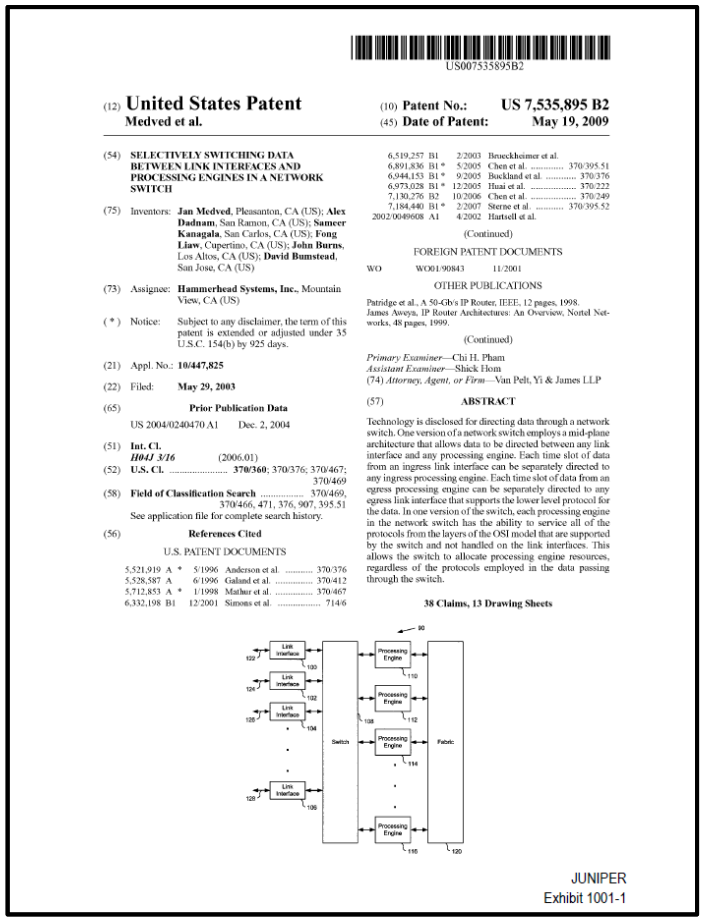
TAL LAVIAN, Ph.D.

APPENDIX A

'895 Patent

The ’895 Patent

The ’895 Patent



US007535895B2

(12) **United States Patent**
Medved et al.

(10) **Patent No.: US 7,535,895 B2**
(45) **Date of Patent: May 19, 2009**

(54) **SELECTIVELY SWITCHING DATA BETWEEN LINK INTERFACES AND PROCESSING ENGINES IN A NETWORK SWITCH**

(75) Inventors: **Jan Medved**, Pleasanton, CA (US); **Alex Dadnam**, San Ramon, CA (US); **Sameer Kanagala**, San Carlos, CA (US); **Fong Liaw**, Cupertino, CA (US); **John Burns**, Los Altos, CA (US); **David Bumstead**, San Jose, CA (US)

(73) Assignee: **Hammerhead Systems, Inc.**, Mountain View, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 925 days.

(21) Appl. No.: **10/447,825**

(22) Filed: **May 29, 2003**

(65) **Prior Publication Data**

US 2004/0240470 A1 Dec. 2, 2004

(51) **Int. Cl.**
H04J 3/16 (2006.01)

(52) **U.S. Cl.** **370/360**; 370/376; 370/467; 370/469

(58) **Field of Classification Search** 370/469, 370/466, 471, 376, 907, 395.51
See application file for complete search history.

(56) **References Cited**

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5,712,853	A *	1/1998	Mathur et al.	370/467
6,332,198	B1	12/2001	Simons et al.	714/6
6,519,257	B1	2/2003	Bruckheimer et al.	
6,891,836	B1 *	5/2005	Chen et al.	370/395.51
6,944,153	B1 *	9/2005	Buckland et al.	370/376
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(Continued)

Primary Examiner—Chi H. Pham
Assistant Examiner—Shick Hom
(74) *Attorney, Agent, or Firm*—Van Pelt, Yi & James LLP

(57) **ABSTRACT**

Technology is disclosed for directing data through a network switch. One version of a network switch employs a mid-plane architecture that allows data to be directed between any link interface and any processing engine. Each time slot of data from an ingress link interface can be separately directed to any ingress processing engine. Each time slot of data from an egress processing engine can be separately directed to any egress link interface that supports the lower level protocol for the data. In one version of the switch, each processing engine in the network switch has the ability to service all of the protocols from the layers of the OSI model that are supported by the switch and not handled on the link interfaces. This allows the switch to allocate processing engine resources, regardless of the protocols employed in the data passing through the switch.

38 Claims, 13 Drawing Sheets

JUNIPER
Exhibit 1001-1

Title: Selectively Switching Data Between Link Interfaces And Processing Engines In A Network Switch

Priority Date: May 29, 2003

Challenged Claims: 5-6 and 14-15

The ’895 Patent

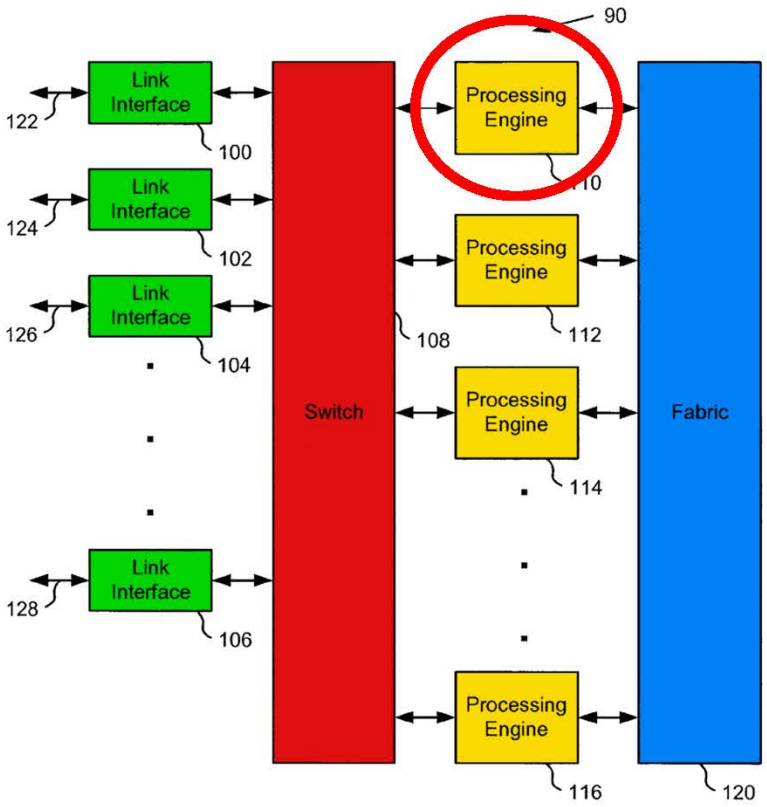


FIG. 1

wherein at least one processing engine in said plurality of processing engines receives data to be processed by said at least one processing engine according to a first protocol within a layer and data to be processed by said at least one processing engine according to a second protocol within said layer and said first protocol is different than said second protocol.

’895 Patent at Fig. 1; *id*. at Multiprotocol Limitation.

The Instituted Ground (Bell + Sierra) Renders the Challenged Claims Obvious

Bell/Sierra Disclose Claimed Network Switch Architecture

’895 Patent

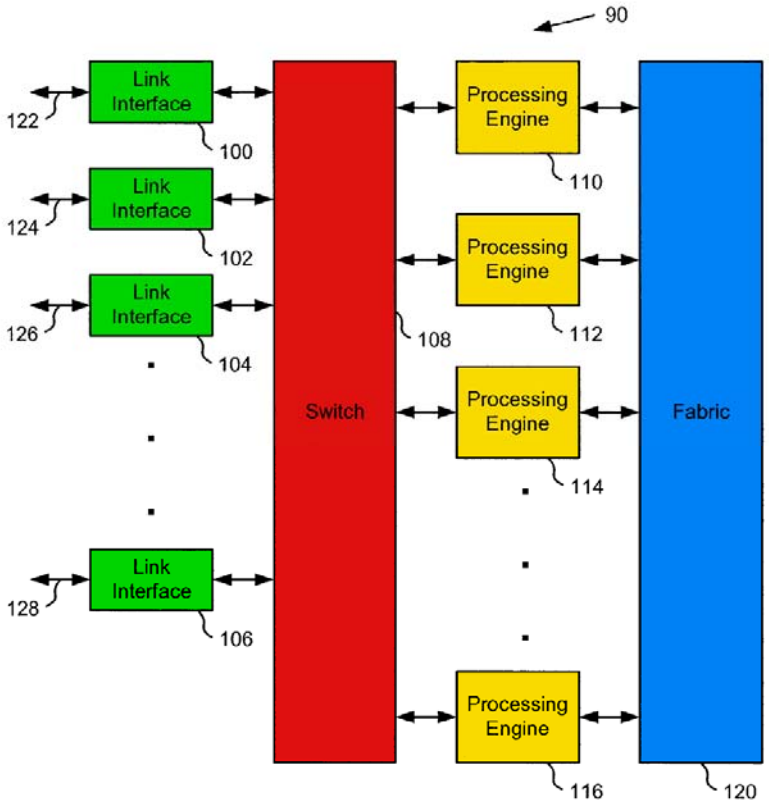


FIG. 1

Bell/Sierra

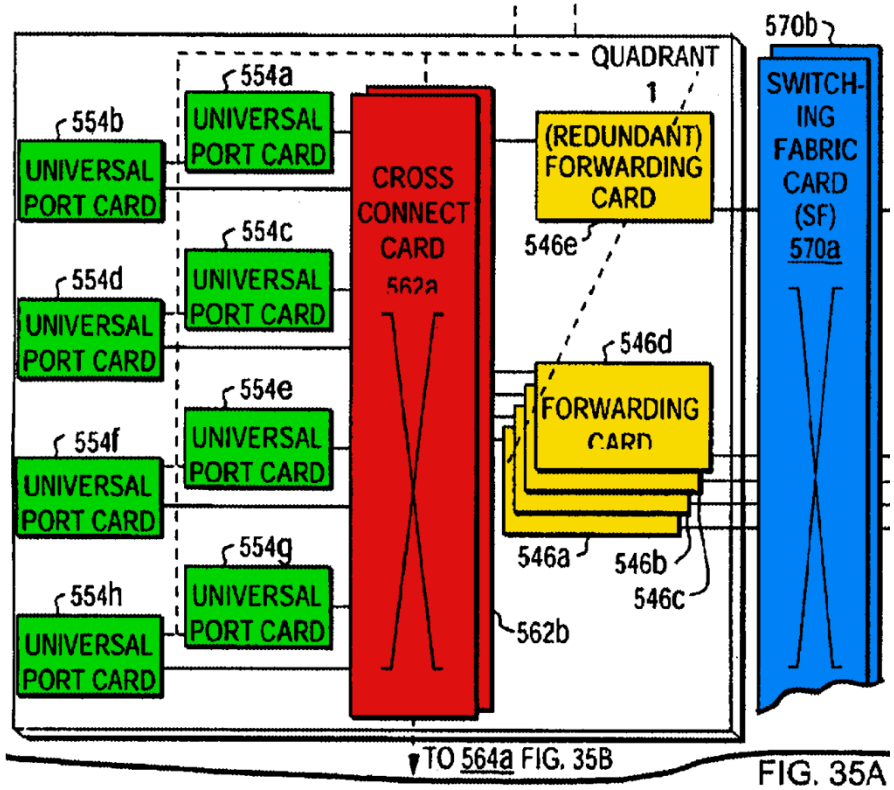


FIG. 35A

’895 Patent at Fig. 1; Bell at Fig. 35A.

Only One Disputed Element

Does Bell Disclose Or Render Obvious A Forwarding Card That Processes Multiple Protocols?

wherein at least one processing engine in said plurality of processing engines receives data to be processed by said at least one processing engine according to a first protocol within a layer and data to be processed by said at least one processing engine according to a second protocol within said layer and said first protocol is different than said second protocol.

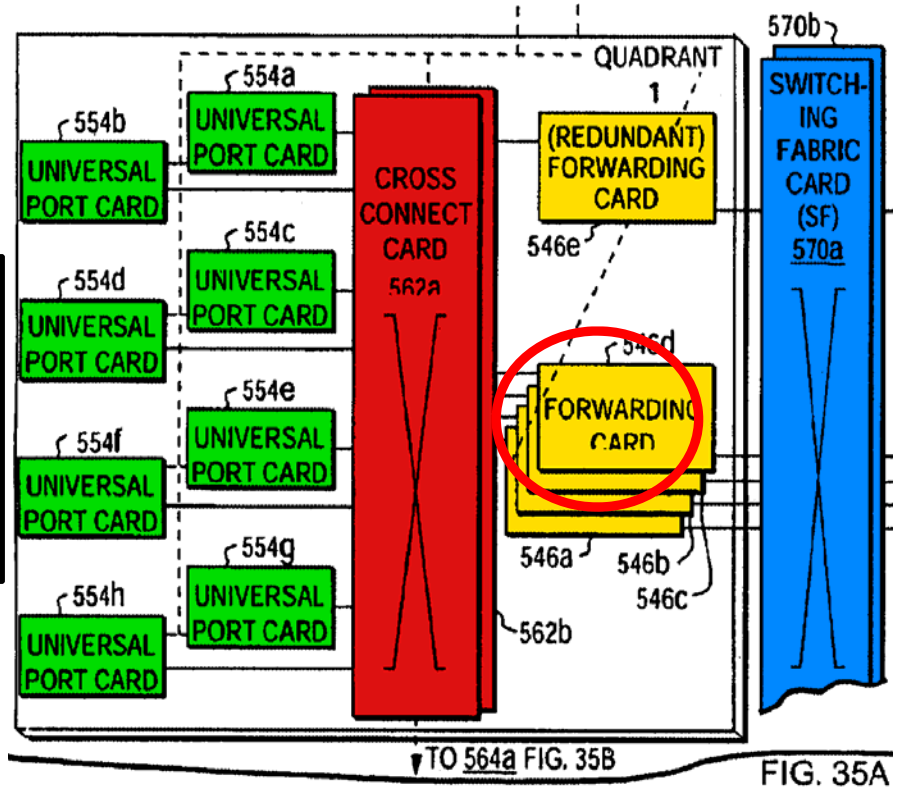
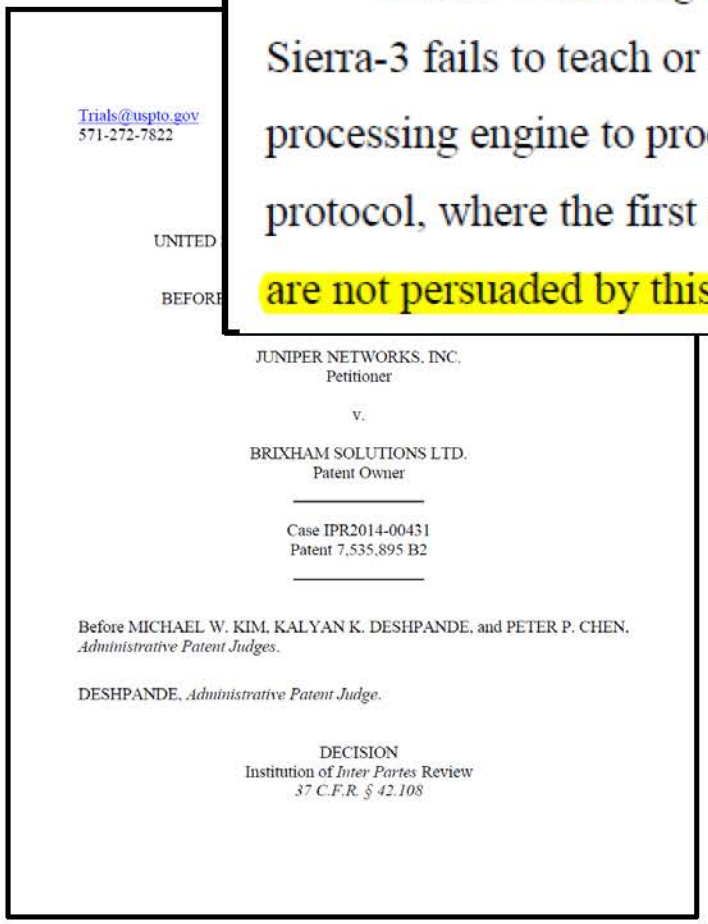


FIG. 35A

'895 Patent at Multiprotocol Limitation; Bell at Fig. 35A.

The Board Already Rejected BSL's Multiprotocol Argument



Trials@uspto.gov
571-272-7822

UNITED

BEFORE

JUNIPER NETWORKS, INC.
Petitioner

v.

BRIXHAM SOLUTIONS LTD.
Patent Owner

Case IPR2014-00431
Patent 7,535,895 B2

Before MICHAEL W. KIM, KALYAN K. DESHPANDE, and PETER P. CHEN,
Administrative Patent Judges.

DESHPANDE, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Patent Owner argues that the combination of Bell, Sierra-1, Sierra-2, and Sierra-3 fails to teach or suggest the multiprotocol limitation that requires the processing engine to process data according to a first protocol and a second protocol, where the first and second protocols are different. Prelim. Resp. 7. We are not persuaded by this argument. In our claim construction above, we do not

Paper 15 at 14.

Bell's Forwarding Cards Process Multiple Protocols

Bell Discloses Or Renders Obvious A Forwarding Card That Processes Multiple Protocols

1. Forwarding Cards Process "Paths" Of Network Data Carrying Different Protocols (*e.g.*, ATM & Frame Relay)

2. *<u>In Addition</u>* To The Paths Of Network Data, Forwarding Cards Process Ethernet "Network Control Information"

Bell Discloses Or Renders Obvious A Forwarding Card That Processes Multiple Protocols

1. Forwarding Cards Process "Paths" Of Network Data Carrying Different Protocols (e.g., ATM & Frame Relay)

2. *<u>In Addition</u>* To The Paths Of Network Data, Forwarding Cards Process Ethernet "Network Control Information"

Link Interfaces Receive "Paths" Of Network Data Carrying Different Protocols

the SONET protocol. Each external network connection may provide multiple streams or paths and each stream or path may include data being transmitted according to a different protocol over SONET. For example, one path may

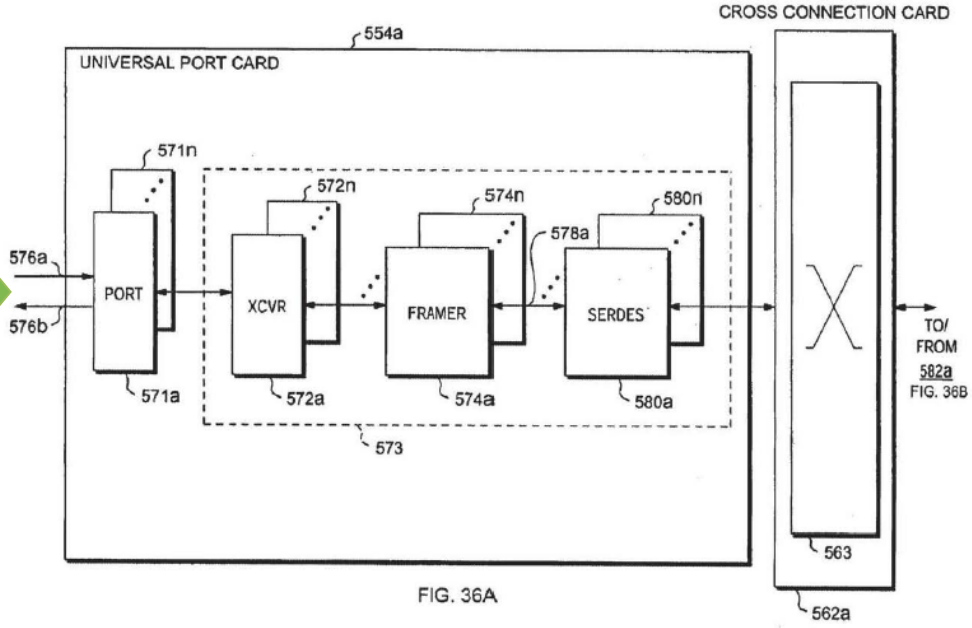
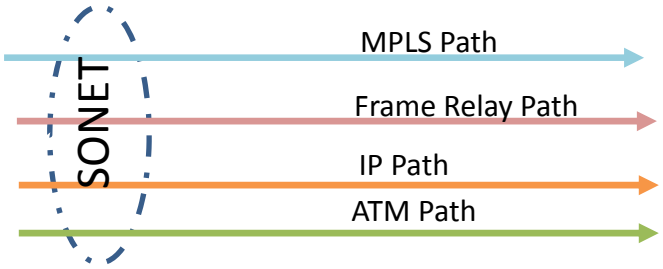
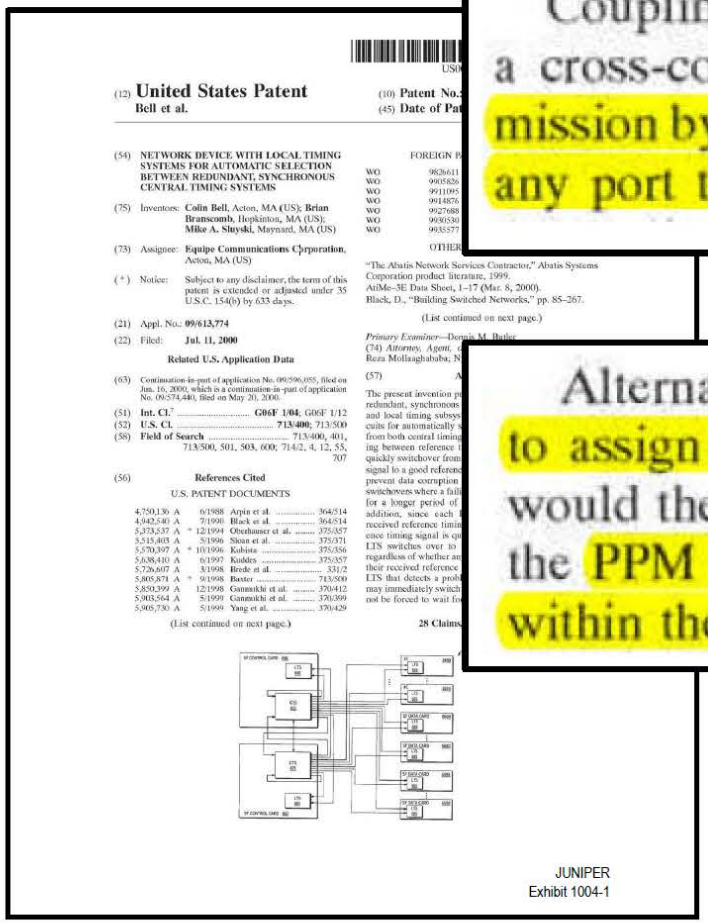


FIG. 36A



Bell at 53:50-56; *id*. at Fig. 36A.

User May Choose Which Forwarding Card To Assign Paths



(12) **United States Patent**
Bell et al.

(10) **Patent No.:**
(45) **Date of Pat**

(54) **NETWORK DEVICE WITH LOCAL TIMING SYSTEMS FOR AUTOMATIC SELECTION BETWEEN REDUNDANT, SYNCHRONOUS CENTRAL TIMING SYSTEMS**

(75) Inventors: **Colin Bell**, Acton, MA (US); **Brian Branscomb**, Hopkinton, MA (US); **Mike A. Shuyski**, Maynard, MA (US)

(73) Assignee: **Equipe Communications Corporation**, Acton, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 633 days.

(21) Appl. No.: **09/613,774**

(22) Filed: **Jul. 11, 2000**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/596,055, filed on Jun. 16, 2000, which is a continuation-in-part of application No. 09/574,440, filed on May 20, 2000.

(51) **Int. Cl.**[7] **G06F 1/04**; G06F 1/12

(52) **U.S. Cl.** **713/400**; 713/500

(58) **Field of Search** 713/400, 401, 713/500, 501, 503, 600; 714/2, 4, 12, 55, 707

(56) **References Cited**

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(List continued on next page.)

Primary Examiner—Dennis M. Butler
(74) *Attorney, Agent,*
Reza Mollaghababa, N

(57) A

The present invention p
redundant, synchronous
and local timing subsys
cuits for automatically
from both central timing
ing between reference
quickly switchover from
signal to a good referen
prevent data corruption
switchovers where a fail
for a longer period of
addition, since each
received reference timi
ence timing signal is qu
LTS switches over to
regardless of whether an
their received reference
LTS that detects a probl
may immediately switch
not be forced to wait fo

28 Claims

JUNIPER
Exhibit 1004-1

Coupling universal port cards to forwarding cards through a cross-connection card provides flexibility in data transmission by allowing data to be transmitted from any path on any port to any port on any forwarding card. In addition,

Alternatively, the user may choose which forwarding card to assign to the new path and notify the NMS. The NMS would then fill in the forwarding card LID in the SET, and the PPM would only determine which time slots and slice within the forwarding card to assign.

Bell at 52:10-14; *id*. at 56:40-45.

A Forwarding Card Can Receive ATM Data

The payload extractor chip also strips off all vestigial SONET frame information and transfers the data path to an ingress interface chip. The ingress interface chip will be specific to the protocol of the data within the path. As one example, the data may be formatted in accordance with the ATM protocol and the ingress interface chip is an ATM interface chip (e.g., ATM IF **584***a*). Other protocols can also be implemented including, for example, Internet Protocol (IP), Multi-Protocol Label Switching (MPLS) protocol or Frame Relay.

ATM Path

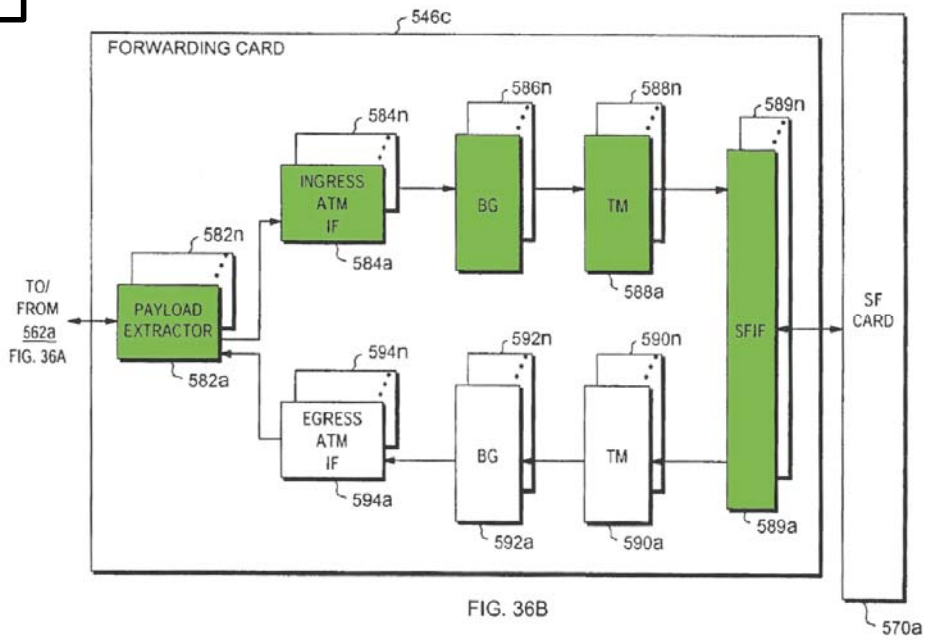


FIG. 36B

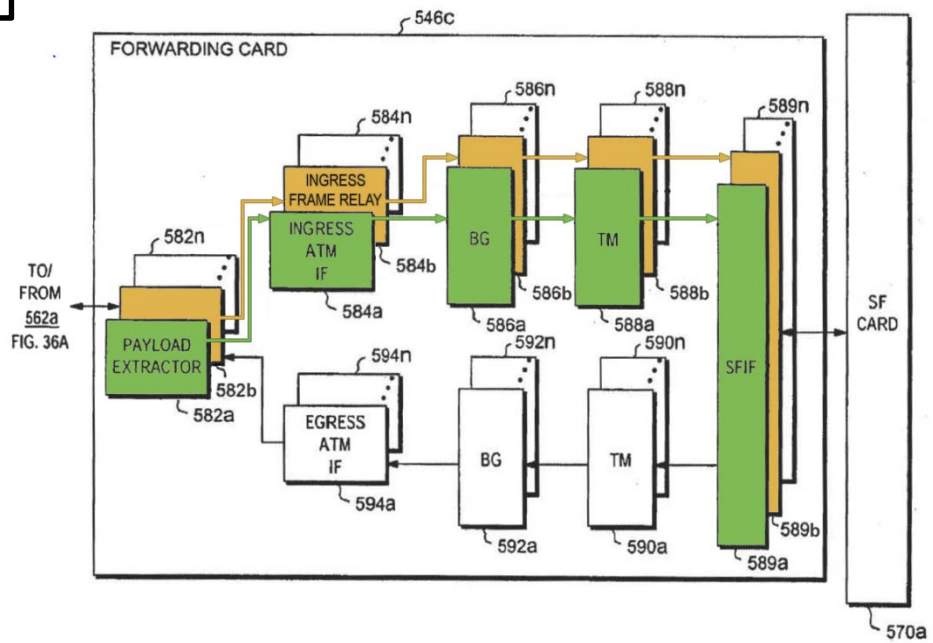
Bell at 50:34-43; *id*. at Fig. 36B.

The Same Forwarding Card Can Receive "Other Protocols" (e.g., Frame Relay)

> The payload extractor chip also strips off all vestigial SONET frame information and transfers the data path to an ingress interface chip. The ingress interface chip will be specific to the protocol of the data within the path. As one example, the data may be formatted in accordance with the ATM protocol and the ingress interface chip is an ATM interface chip (e.g., ATM IF **584***a*). Other protocols can also be implemented including, for example, Internet Protocol (IP), Multi-Protocol Label Switching (MPLS) protocol or Frame Relay.

Frame Relay Path

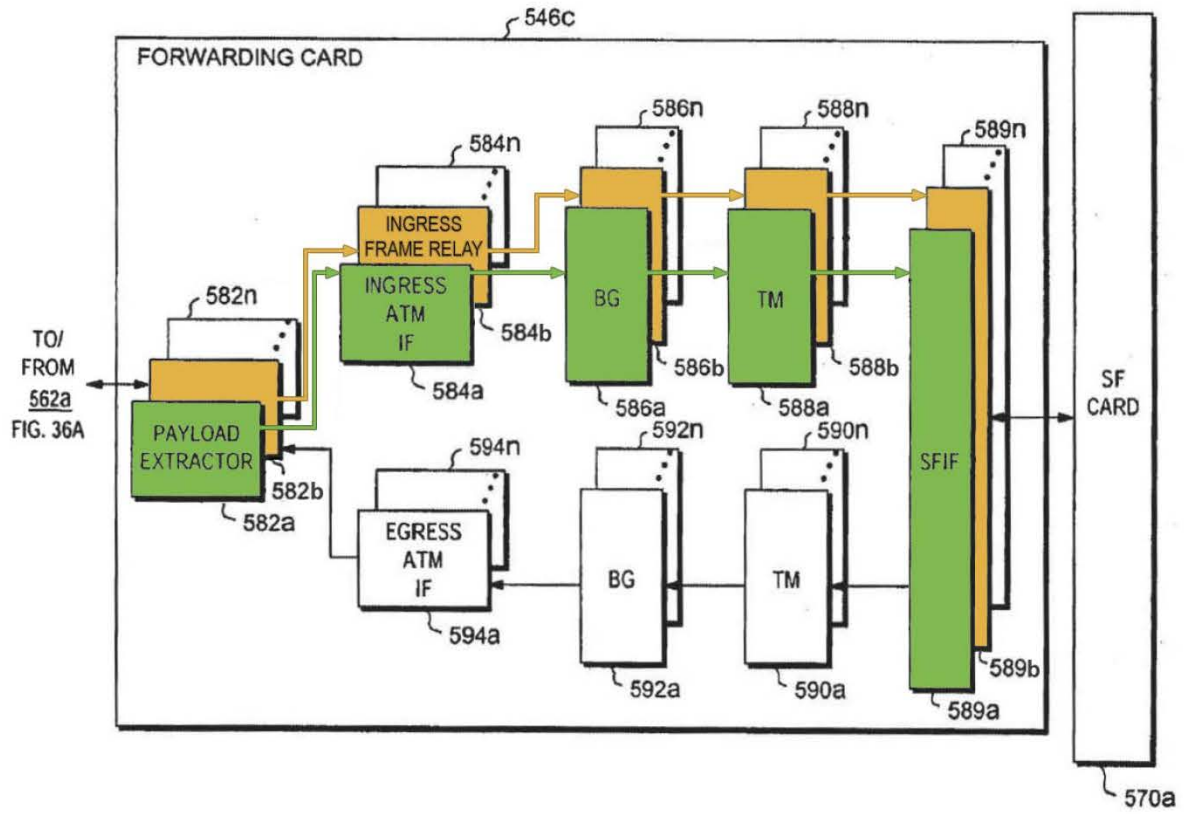
ATM Path



Bell at 50:34-43; *id*. at Fig. 36B (modified to show Frame Relay route).

Dr. Lavian: Obvious To Use Different Protocol Interface Chips On A Forwarding Card

INGRESS FRAME RELAY



Bell at Fig. 36B (modified to show Frame Relay route)

Obvious To Use Different Protocol Interface Chips On A Forwarding Card

"When a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious."

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 417 (2007) (internal citations omitted).

Bell Discloses Or Renders Obvious A Forwarding Card That Processes Multiple Protocols

1. Forwarding Cards Process "Paths" Of Network Data Carrying Different Protocols (e.g., ATM & Frame Relay)

2. *In Addition* To The Paths Of Network Data, Forwarding Cards Process Ethernet "Network Control Information"

Each Forwarding Cards Is Connected To An Ethernet Bus

and eight universal port cards (e.g., **554***a*–**554***h*). Network device **540** is a distributed processing system. Each of the cards includes a processor and is connected to the Ethernet control bus. In addition, each of the cards are configured as described above with respect to line cards.

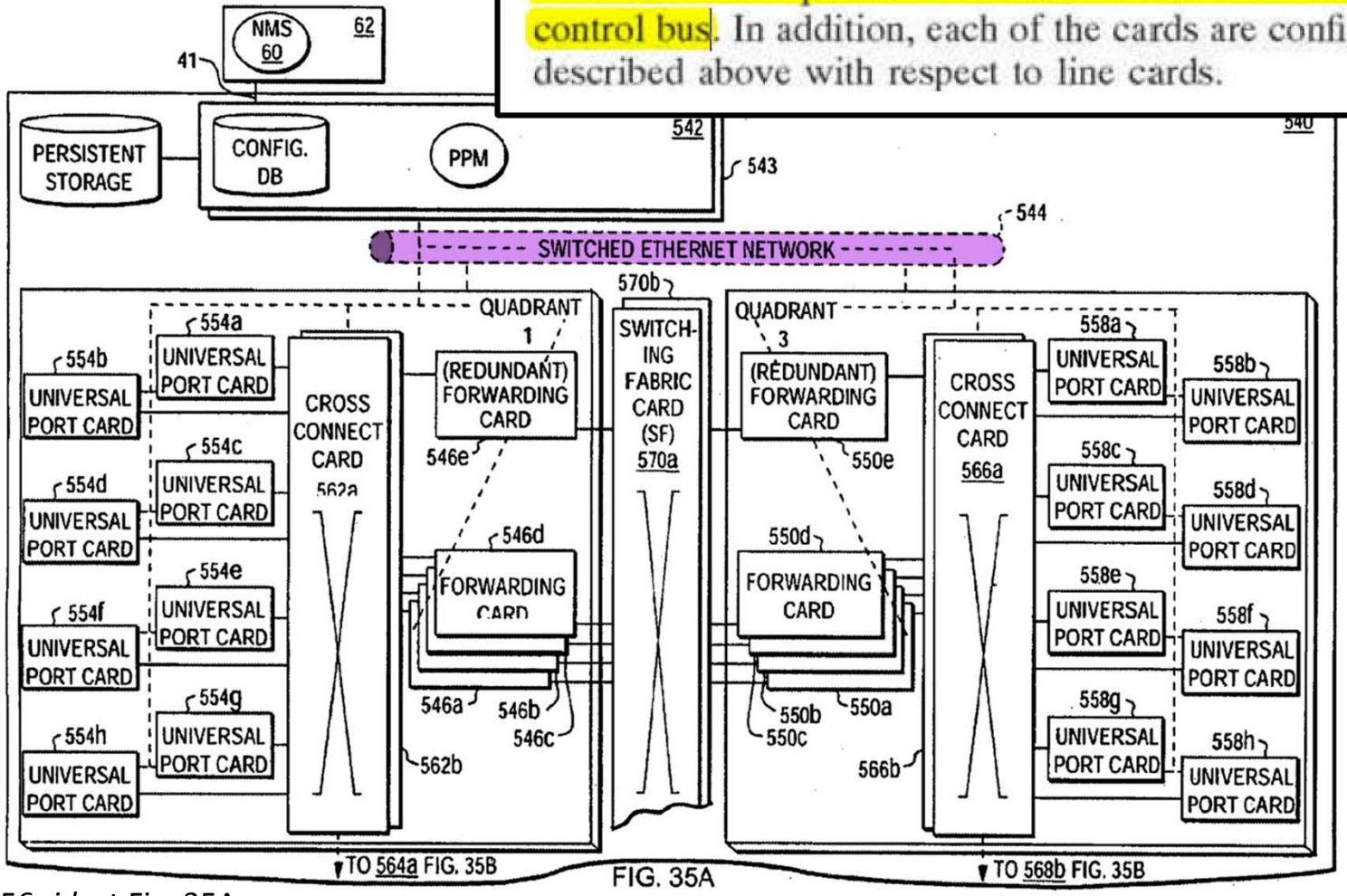


FIG. 35A

Bell at 48:54-56; *id*. at Fig. 35A.

Each Forwarding Card Processes Ethernet "Network Control Information"

network control information. The forwarding card itself processes certain network control information and sends certain other network control information to the central processor over the Fast Ethernet control bus. The forwarding card also generates network control payloads and receives network control payloads from the central processor. The

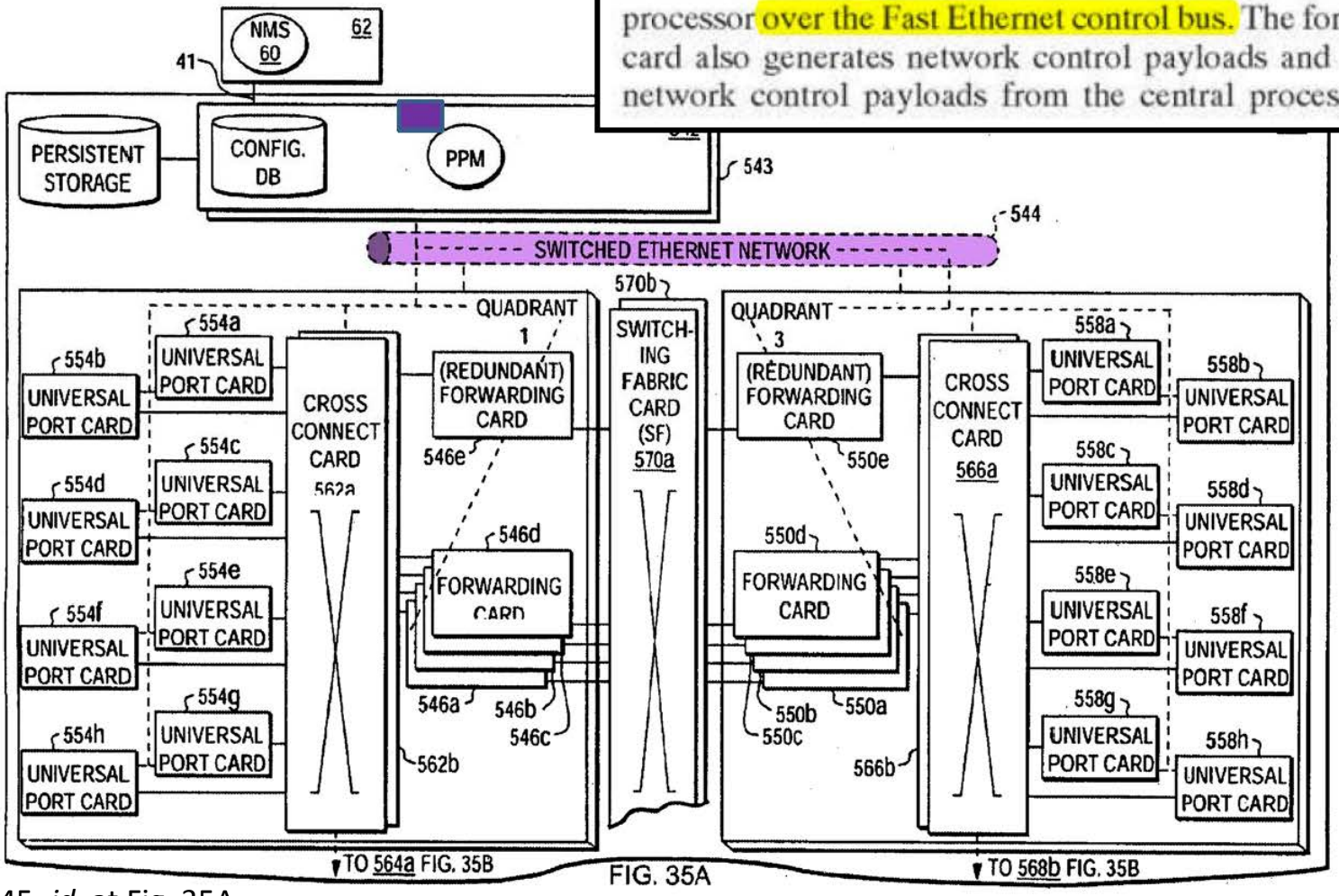


FIG. 35A

Bell at 49:39-45; *id*. at Fig. 35A.

The Ethernet Data Is *In Addition* To The Network Data The Forwarding Card Processes

network control information. The forwarding card itself processes certain network control information and sends certain other network control information to the central processor over the Fast Ethernet control bus. The forwarding card also generates network control payloads and receives network control payloads from the central processor. The

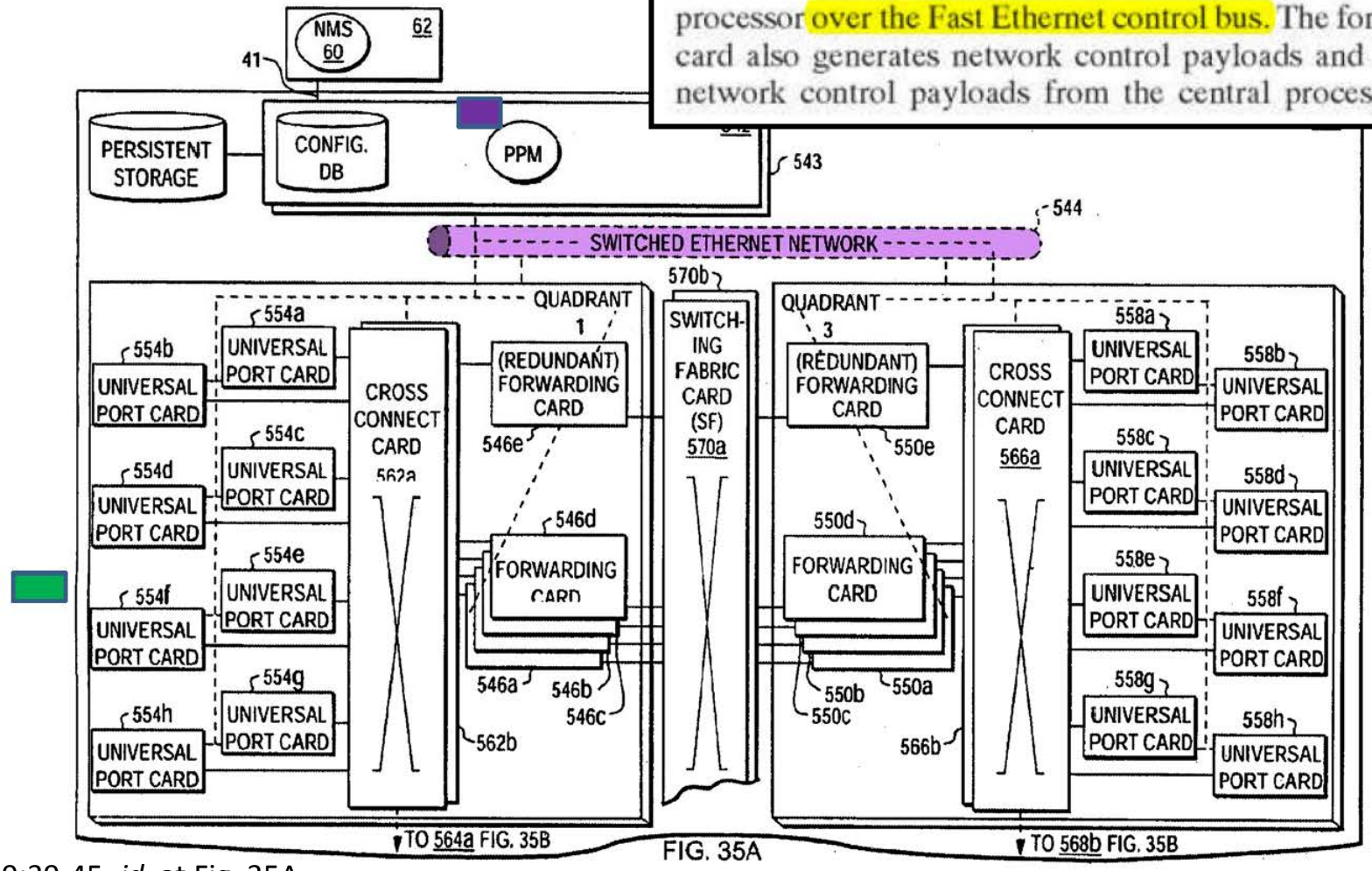
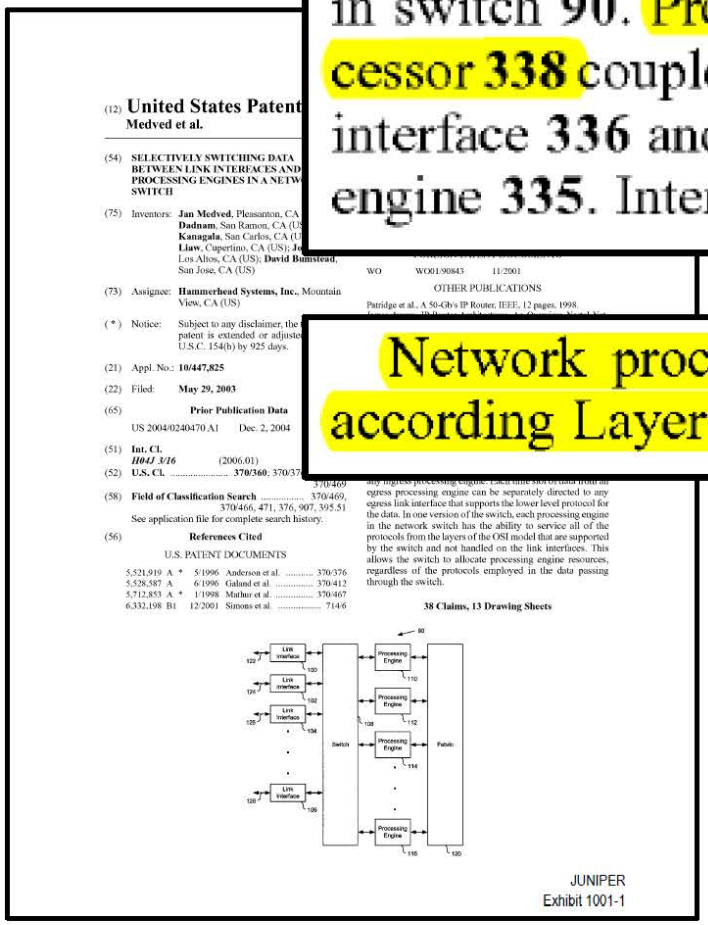


FIG. 35A

Bell at 49:39-45; *id*. at Fig. 35A.

Bell Renders Obvious The Multiprotocol Limitation

Claimed Processing Engine Employs A Network Processor



(12) **United States Patent**
Medved et al.

(54) **SELECTIVELY SWITCHING DATA BETWEEN LINK INTERFACES AND PROCESSING ENGINES IN A NETW SWITCH**

(75) Inventors: **Jan Medved**, Pleasanton, CA; **Dadnam**, San Ramon, CA (US); **Kanagala**, San Carlos, CA (US); **Liaw**, Cupertino, CA (US); **Jo** Los Altos, CA (US); **David Bamstead**, San Jose, CA (US)

(73) Assignee: **Hammerhead Systems, Inc.**, Mountain View, CA (US)

(*) Notice: Subject to any disclaimer, the patent is extended or adjuste U.S.C. 154(b) by 925 days.

(21) Appl. No.: **10/447,825**

(22) Filed: **May 29, 2003**

(65) **Prior Publication Data**

US 2004/0240470 A1 Dec. 2, 2004

(51) **Int. Cl.**
H04J 3/16 (2006.01)

(52) **U.S. Cl.** **370/360**; 370/37

370/469

(58) **Field of Classification Search** 370/469, 370/466, 471, 376, 907, 395.51
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

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5,528,587	A	6/1996	Galand et al.	370/412
5,712,853	A *	1/1998	Mathur et al.	370/467
6,332,198	B1	12/2001	Simons et al.	714/6

WO WO01/90843 11/2001

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Patridge et al., A 50-Gb/s IP Router, IEEE, 12 pages, 1998.

egress processing engine can be separately directed to any egress link interface that supports the lower level protocol for the data. In one version of the switch, each processing engine in the network switch has the ability to service all of the protocols from the layers of the OSI model that are supported by the switch and not handled on the link interfaces. This allows the switch to allocate processing engine resources, regardless of the protocols employed in the data passing through the switch.

38 Claims, 13 Drawing Sheets

JUNIPER
Exhibit 1001-1

in switch **90**. Processing engine **110** includes network processor **338** coupled to exchange information with fabric plane interface **336** and switch plane interface **342** via conversion engine **335**. Interface **342** is coupled to switch plane **152** to

Network processor **338** processes data from plane **152** according Layer 2 protocols and above. Network processor

'895 patent at 21:42-44; *id*. at 21:58-60.

Dr. Lavian: Obvious To Employ A Network Processor In Bell

Dr. Tal Lavian
UC Berkeley

- Network Processors Were:
  - ✓ Well-Known Off-The-Shelf Components
  - ✓ Could Handle Multiple Protocols
  - ✓ Ideally Suited For Bell's Forwarding Cards
- Employing A Network Processor Was Well Within The Capabilities Of A PHOSITA

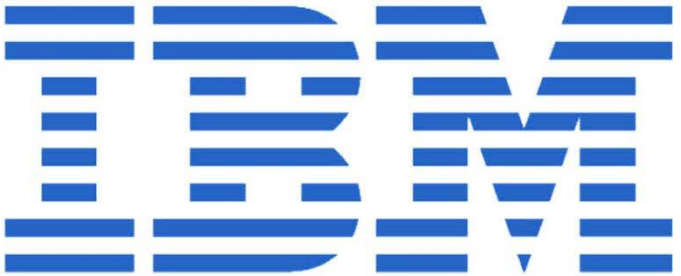
Ex. 1020, ¶¶ 37-57.

Dr. Lavian's Testimony Stands Unrebutted

BSL Does Not Identify:

- Any reason why employing a network processor on Bell's forwarding cards would not render obvious the multiprotocol limitation
- Any reason why a PHOSITA could not employ a network processor on Bell's forwarding cards
- Any alleged difficulties a PHOSITA would have in employing a network processor on Bell's forwarding cards
- Any disclosure that teach away from employing a network processor on Bell's forwarding cards

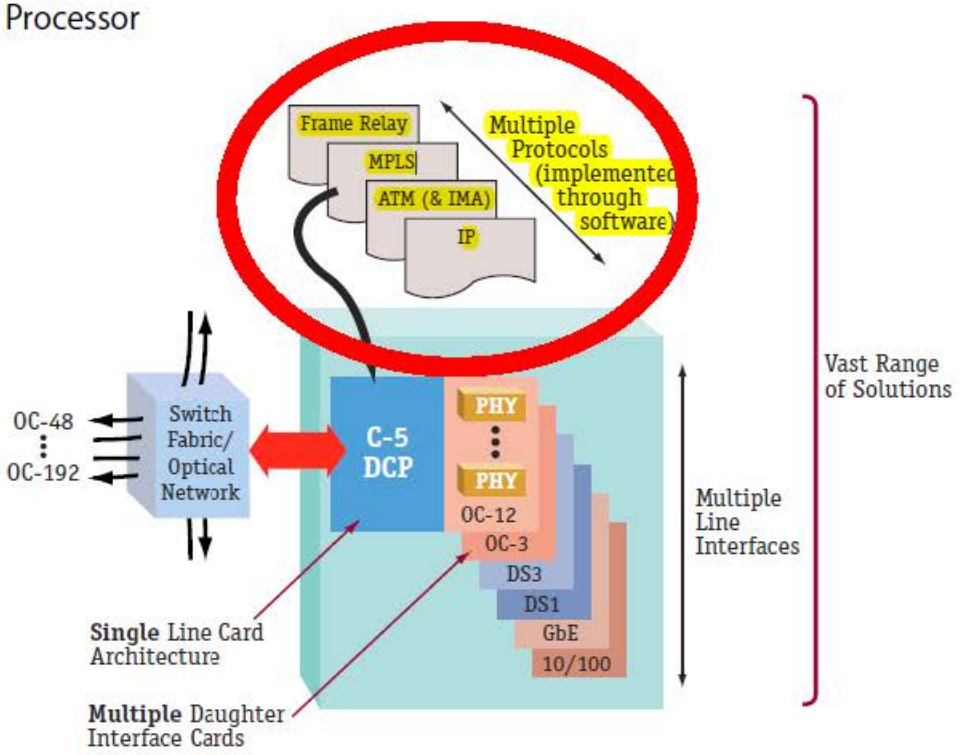
Network Processors Were Known & Available Off-The-Shelf



Ex. 1020, ¶ 39.

Network Processors Handled Multiple Protocols

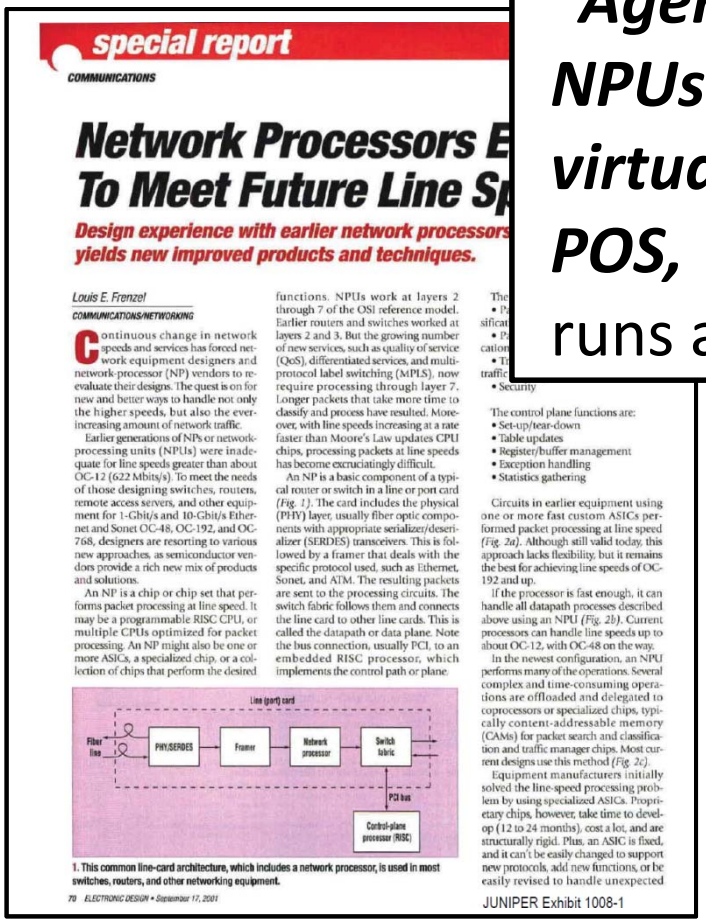
Figure 2 Universal Switch-Router Line Cards Based on Network Processor



This type of multiprotocol solution offers important time-to-market competitive advantages, and dramatically reduces support costs for both the network vendor and service provider.

Ex. 1003, App. 18 at 2.

Agere Chip Sets Were Popular And Handled Virtually Any Protocol



special report

COMMUNICATIONS

Network Processors E
To Meet Future Line Sp

Design experience with earlier network processors yields new improved products and techniques.

Louis E. Frenzel

COMMUNICATIONS/NETWORKING

Continuous change in network speeds and services has forced network equipment designers and network-processor (NP) vendors to re-evaluate their designs. The quest is on for new and better ways to handle not only the higher speeds, but also the ever-increasing amount of network traffic.

Earlier generations of NPs or network-processing units (NPUs) were inadequate for line speeds greater than about OC-12 (622 Mbits/s). To meet the needs of those designing switches, routers, remote access servers, and other equipment for 1-Gbit/s and 10-Gbit/s Ethernet and Sonet OC-48, OC-192, and OC-768, designers are resorting to various new approaches, as semiconductor vendors provide a rich new mix of products and solutions.

An NP is a chip or chip set that performs packet processing at line speed. It may be a programmable RISC CPU, or multiple CPUs optimized for packet processing. An NP might also be one or more ASICs, a specialized chip, or a collection of chips that perform the desired functions. NPUs work at layers 2 through 7 of the OSI reference model. Earlier routers and switches worked at layers 2 and 3. But the growing number of new services, such as quality of service (QoS), differentiated services, and multi-protocol label switching (MPLS), now require processing through layer 7. Longer packets that take more time to classify and process have resulted. Moreover, with line speeds increasing at a rate faster than Moore's Law updates CPU chips, processing packets at line speeds has become excruciatingly difficult.

An NP is a basic component of a typical router or switch in a line or port card (*Fig. 1*). The card includes the physical (PHY) layer, usually fiber optic components with appropriate serializer/deserializer (SERDES) transceivers. This is followed by a framer that deals with the specific protocol used, such as Ethernet, Sonet, and ATM. The resulting packets are sent to the processing circuits. The switch fabric follows them and connects the line card to other line cards. This is called the datapath or data plane. Note the bus connection, usually PCI, to an embedded RISC processor, which implements the control path or plane.

1. This common line-card architecture, which includes a network processor, is used in most switches, routers, and other networking equipment.

• Security

The control plane functions are:
• Set-up/tear-down
• Table updates
• Register/buffer management
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• Statistics gathering

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If the processor is fast enough, it can handle all datapath processes described above using an NPU (*Fig. 2b*). Current processors can handle line speeds up to about OC-12, with OC-48 on the way.

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Equipment manufacturers initially solved the line-speed processing problem by using specialized ASICs. Proprietary chips, however, take time to develop (12 to 24 months), cost a lot, and are structurally rigid. Plus, an ASIC is fixed, and it can't be easily changed to support new protocols, add new functions, or be easily revised to handle unexpected

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JUNIPER Exhibit 1008-1

"***Agere Systems is a major player in NPUs***. . . . The chip set handles ***virtually any type of traffic—SONET, POS, Frame Relay, ATM, MPLS***—and runs at OC-48 speed."

Ex. 1008-2.

Bell Was The Target Application For A Network Processor

agere systems

10G Network Processor Chip Set (APP750NP ar

Introduction

The Agere Systems *PayloadPlus*® 10G Network Processor chip set provides wire-speed deep-packet processing for high performance packet-processing systems. This software-compatible, programmable chip set consists of two chips—the APP750NP classification engine (NP10) and the APP750TM traffic manager (TM10)—and follows the successful Agere Systems 2.5G *PayloadPlus* chip set.

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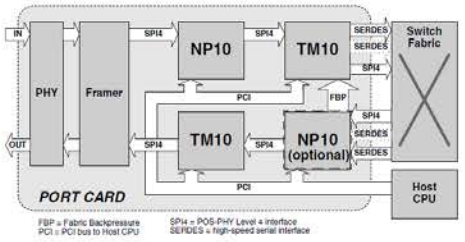
The chip set supp
classification pol
IPv6 classification, PPPoE, L2TP, MPLS, etc., with a large amount of headroom for future classification needs. OEMs use the Agere Systems high-level Functional Programming Language (FPL) to specify packet classification policies. Statistics, policing, and packet modification functions are performed by on-chip compute engines that are programmed using the C-like Agere Scripting Language (ASL).



10G Network Processor System Diagram

JUNIPER
Exhibit 1009-1

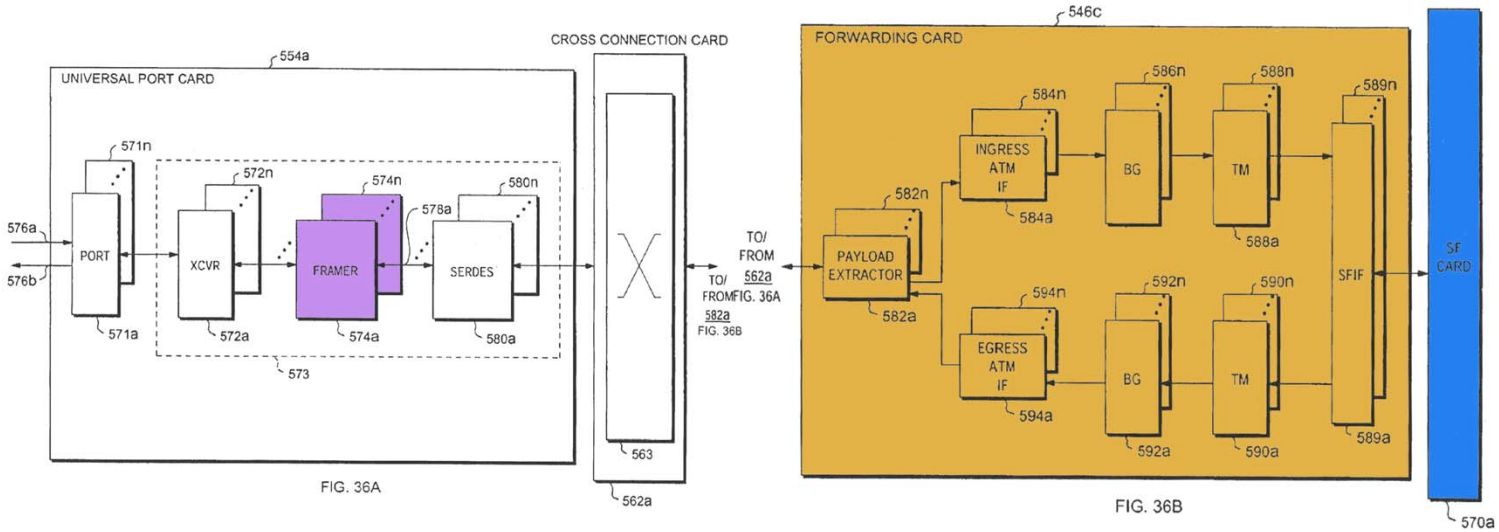
Applications

Target applications include multiprotocol core and edge switches and routers, multiservice optical core and edge devices and service-aware switches and provisioning platforms.

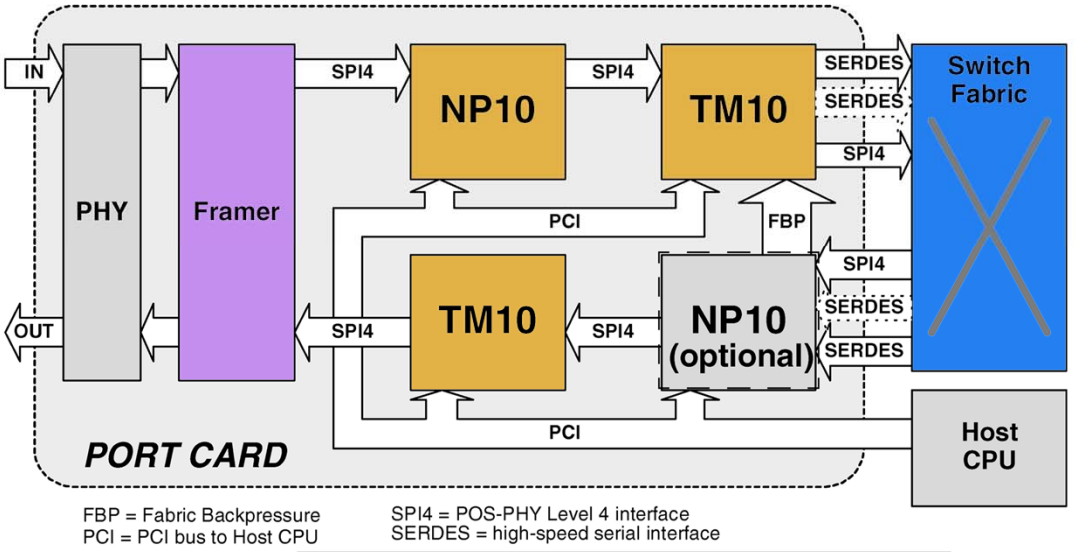
Ex. 1009-2.

Bell's Forwarding Cards Were Ideally Suited For A Network Processor

Bell
Forwarding Card
Fits Between
Framer And
Switch Fabric



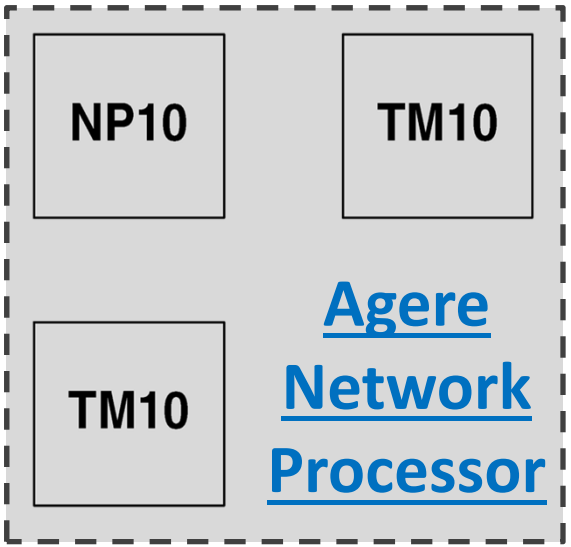
NP Architecture
Network Processors
Designed To Fit
Between Framer
And Switch Fabric



10G Network Processor System Diagram

Ex. 1020, ¶¶ 44-46.

Employing A Network Processor Was Simple Substitution



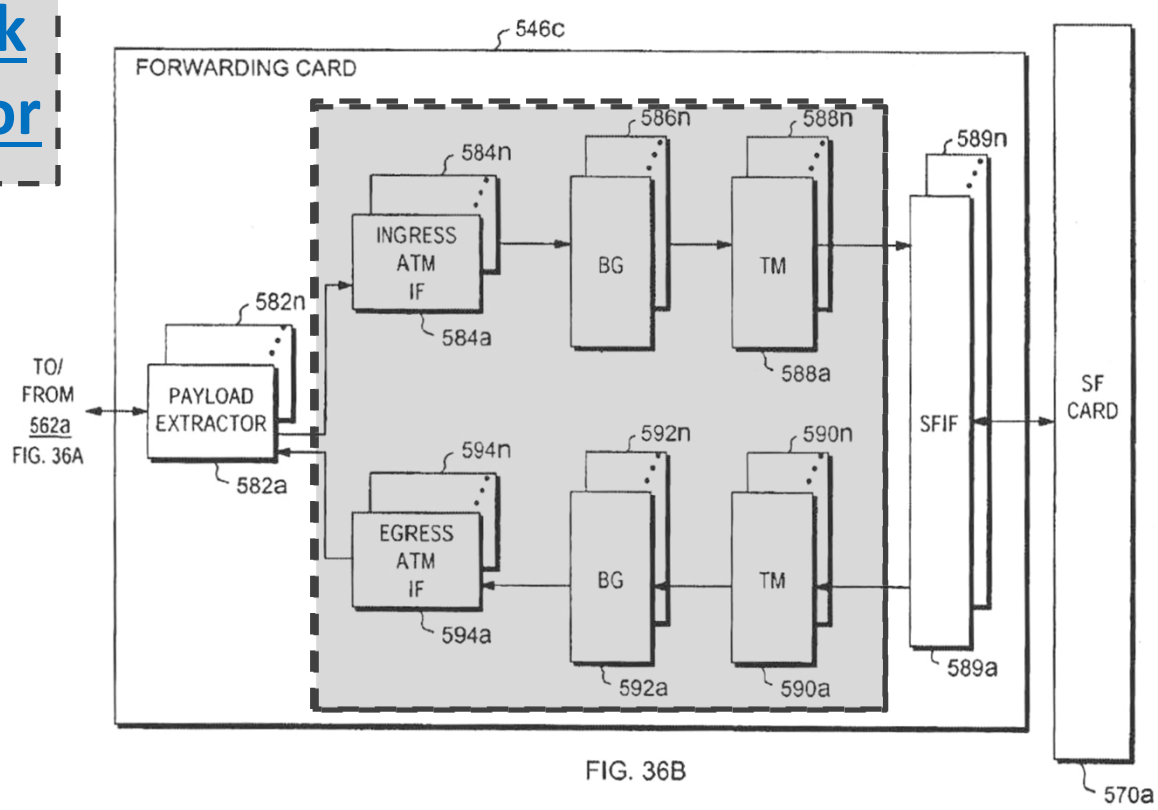


FIG. 36B

Ex. 1020, ¶ 42.

Numerous Exemplary Rationales From *KSR*/MPEP Apply

A **Combining prior art elements according to known methods to yield predictable results**

B Simple Substitution of One Known Element for Another To Obtain Predictable Results

C Use of known technique to improve similar devices in the same way

G Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or combine prior art reference teachings to arrive at the claimed invention

Exemplary Rationale A

Combining prior art elements according to known methods to yield predictable results

Dr. Tal Lavian
UC Berkeley

Combining the elements of **Bell's network switch** with the element of **a multiprotocol network processor**, according to known methods of **network design**, yields the predictable result of **a network switch that can efficiently handle any protocol**.

Ex. 1020, ¶ 50.

Numerous Exemplary Rationales From *KSR*/MPEP Apply

A. Combining prior art elements according to known methods to yield predictable results

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Exemplary Rationale B

Simple substitution of one known element for another to obtain predictable results

Dr. Tal Lavian
UC Berkeley

Simple substitution of **Bell's interface, bridge and traffic management chips** for **a multiprotocol network processor** to obtain the predictable result of **a network switch that can efficiently handle any protocol**.

Ex. 1020, ¶ 51.

Numerous Exemplary Rationales From *KSR*/MPEP Apply

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B. Simple substitution of one known element for another to obtain predictable results

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Exemplary Rationale C

Use of known techniques to improve similar devices in the same way

Dr. Tal Lavian
UC Berkeley

Use of **multiprotocol network processors** to improve **handling of multiple protocols** in **network switches like Bell**.

Ex. 1020, ¶ 52.

Network Processors Improve Handling Of Multiple Protocols

special report

COMMUNICATIONS

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Louis E. Frenzel
COMMUNICATIONS/NETWORKING

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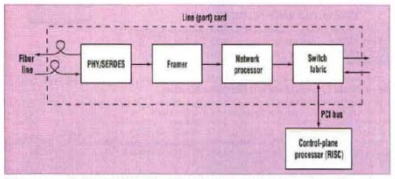

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• Packet processing or data modification
• Traffic or queue management and traffic shaping
• Security

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Equipment manufacturers initially solved the line-speed processing problem by using specialized ASICs. Proprietary chips, however, take time to develop (12 to 24 months), cost a lot, and are structurally rigid. Plus, an ASIC is fixed, and it can't be easily changed to support new protocols, add new functions, or be easily revised to handle unexpected

"ASIC is fixed, and it can't be easily changed to support new protocols. . . The network processor was developed to solve this problem."

Ex. 1008-2.

Numerous Exemplary Rationales From *KSR*/MPEP Apply

A. Combining prior art elements according to known methods to yield predictable results

B. Simple substitution of one known element for another to obtain predictable results

C. Use of known technique to improve similar devices in the same way

G. Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or combine prior art reference teachings to arrive at the claimed invention

Exemplary Rationale G

Teachings, suggestions, or motivations in Bell and the knowledge generally available to a PHOSITA that would have led a PHOSITA to modify Bell to arrive at the claimed invention

Dr. Tal Lavian
UC Berkeley

- **Network Processor furthers Bell's express goals of:**
  - ✓ **Providing "flexibility for future network device changes" and "different needs of different users/customers."**
  - ✓ **Allowing data to be directed "between any of the forwarding cards"**

Ex. 1020, ¶¶ 55-56.

Exemplary Rationale G

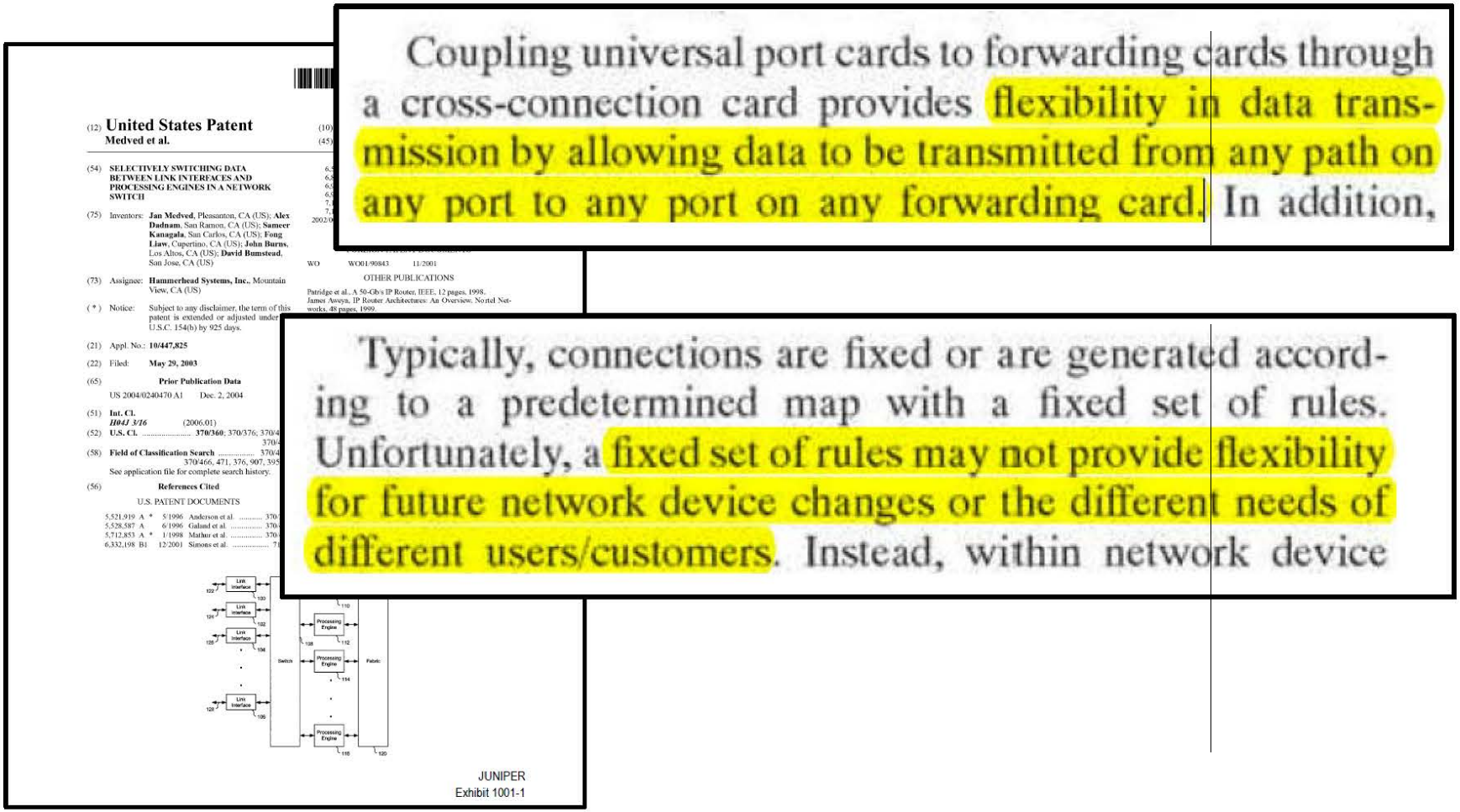
Teachings, suggestions, or motivations in Bell and the knowledge generally available to a PHOSITA that would have led a PHOSITA to modify Bell to arrive at the claimed invention

Dr. Tal Lavian
UC Berkeley

- **Network Processor provides numerous benefits for multiprotocol switches, including:**
  - ✓ **Flexibility and performance**
  - ✓ **Ability to add new protocols and functions that suit different customers needs**
- **Multiprotocol switches like Bell are the "target application" for network processors**

Ex. 1020, ¶¶ 55-56.

Bell's Goal: Increased System Flexibility



(12) **United States Patent**
Medved et al.

(54) **SELECTIVELY SWITCHING DATA BETWEEN LINK INTERFACES AND PROCESSING ENGINES IN A NETWORK SWITCH**

(75) Inventors: **Jan Medved**, Pleasanton, CA (US); **Alex Dadnam**, San Ramon, CA (US); **Sameer Kanagala**, San Carlos, CA (US); **Fong Liaw**, Cupertino, CA (US); **John Burns**, Los Altos, CA (US); **David Bumstead**, San Jose, CA (US)

(73) Assignee: **Hammerhead Systems, Inc.**, Mountain View, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under U.S.C. 154(b) by 925 days.

(21) Appl. No.: **10/447,825**

(22) Filed: **May 29, 2003**

(65) **Prior Publication Data**

US 2004/0240470 A1 Dec. 2, 2004

(51) **Int. Cl.**
H04J 3/16 (2006.01)

(52) **U.S. Cl.** **370/360**; 370/376; 370/4
370/4

(58) **Field of Classification Search** 370/4
370/466, 471, 376, 907, 395
See application file for complete search history.

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WO WO01/90843 11/2001

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JUNIPER
Exhibit 1001-1

Coupling universal port cards to forwarding cards through a cross-connection card provides flexibility in data transmission by allowing data to be transmitted from any path on any port to any port on any forwarding card. In addition,

Typically, connections are fixed or are generated according to a predetermined map with a fixed set of rules. Unfortunately, a fixed set of rules may not provide flexibility for future network device changes or the different needs of different users/customers. Instead, within network device

Bell at 52:10-14; *id*. at 54:50-55.

Network Processors Provide Maximum System Flexibility

Freescale Semiconductor,

Network Processors
A Definition and C

C-PORT.
A Motorola Company

Freescale Semiconductor, Inc.

By: David Husak
C-Port Founder and
Chief Technical Officer

White Paper

A growing class of communications silicon, the
revolutionize how networking vendors architec
Network Processors deliver dramatic improvem
and system capabilities. This paper examines th
comparison to other networking silicon offerin

A Brief History of Network Prod

The design of networking products has undergo
functionality of local and wide-area networks h
packet-based networking, networking devices
with a combination of general purpose CPUs, d
Specific Standard Products), including interface
software-based nature of these devices was key
and the additional functionality required by net
these designs were large, complex, and compar
early networks (generally comprised of a few Et
slow (56kbps) wide-area links).

Over time, as network interface speeds and der
general-purpose processors fell short of what A
develop simpler, fixed-function devices (such a
built with ASICs (Application Specific Integrated
programmability of software-based designs for
technology progressed (and vendors invested h
teams), more and more functionality was incorp
enabled in part by protocol consolidation arour
enterprise network technology, which reduced

The relative simplification of network products
"commoditize" some networking segments thr
Ethernet "switch-on-a-chip" products. Some of
functionality within a narrow range of applicati
Ethernet/IP switching. However, network vendo
still required long and risky internal ASIC devel

Today's Network System Develop

"It's the software, stupid!"
Vint Cerf, Senior VP for Internet Architecture and Technology MCI WorldCom, and "Father of the Internet"
ComSec Seminar, January 1999

Today, the convergence of public voice and data networks is speeding up the pace of change in the communications industry. This is leading to increased time-to-market pressure and shorter product lifecycles — just when product development cycles are growing due to complex ASIC designs and associated software re-designs.

Although IP is emerging as the dominant protocol, newly defined IP capabilities, such as Quality of Service (QoS) and Multiprotocol Label Switching (MPLS), require vendors to continually support new applications. In addition, the number of different interface types,

For More Information On This Product,
Go to: www.freescale.com

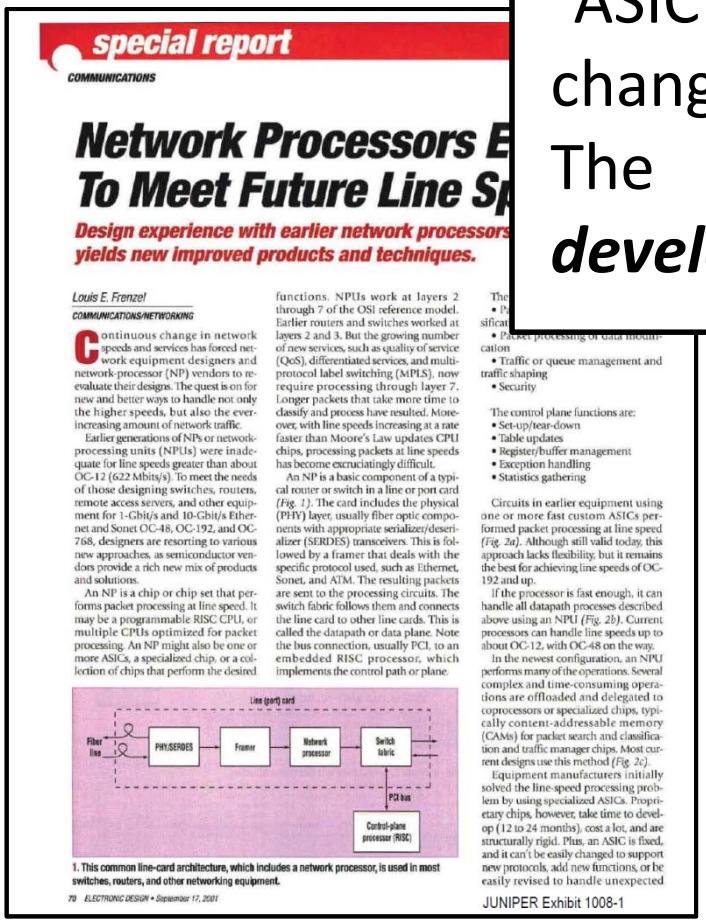
JUNIPER Exhibit 1003
App. 18, pg. 1

Table 1 Network Processor's Seven Key Attributes

Attribute	Benefit
Complete programmability	Supports universal networking applications
A simple programming model	Leads to faster time-to-market
Maximum system flexibility	Enables longer time-in-market™
Massive processing power	Provides scalable performance
High functional integration	Lowers total system costs
Open programming interfaces	Delivers higher availability
Third-party support	Encourages continuous innovation in the industry

Ex. 1003, App. 18 at 2.

Network Processors Provide Maximum System Flexibility



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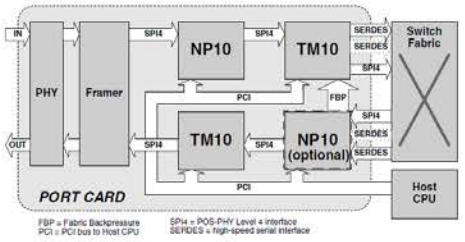

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'895 Patent